NBTI/PBTI-Aware Wordline Voltage Control with No Boosted Supply for Stability Improvement of Half-Selected SRAM Cells

Zhao Chuan Lee, Kim Ming Ho, Zhi Hui Kong, and Tony T. Kim
VIRTUS, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798, E-mail: e110002@ntu.edu.sg, zhkong@ntu.edu.sg, thkim@ntu.edu.sg

Abstract—Negative Bias Temperature Instability (NBTI) and Positive Bias Temperature Instability (PBTI) are the two important reliability issues that degrade the SRAM cell stability over time. In this paper, we analyze the impact of NBTI and PBTI on 8T SRAM cells, and propose a stability improvement technique without using boosted supply voltage. In decoupled SRAM cells, the cell stability is limited by the stability of the half-selected cells, whose stability is significantly affected by NBTI and PBTI. The proposed technique lowers the WWL voltage to reduce the amount of disturbance and compensate the degraded cell stability. Lowering the WWL voltage doesn’t affect the write margin substantially since the write margin is improved with NBTI and PBTI and the lowered WWL will produce a write margin similar to the original one.

Keywords-Negative Bias Temperature Instability (NBTI), Positive Bias Temperature Instability (PBTI), Write Half-Selected Static Noise Margin (HS-SNM), Write Margin (WM)

I. INTRODUCTION

Negative Bias Temperature Instability (NBTI) and Positive Bias Temperature Instability (PBTI) are the two well-known circuit reliability issues in the semiconductor devices. The NBTI in PMOS transistors and the PBTI in the NMOS transistors occur when the transistors are biased in the strong inversion region. The NBTI and PBTI stresses cause the threshold voltage ($V_{th}$) of transistors drift strongly depending on the stress time and stress condition. This degrades the transistor performance over time. NBTI has been dominant in the poly-gate CMOS technologies. However, both NBTI and PBTI still exist in the high-k metal gate process [1-2].

In the state-of-the-art Static Random Access Memory (SRAM) design, SRAM cells are always optimized to meet the desired performance and stability requirement. However, the targeted performance and stability at the initial state will be affected by the NBTI and PBTI degradation over time and eventually lead to circuit failure. Furthermore, the degraded cell stability caused by NBTI and PBTI becomes worse in highly scaled technologies [3-5]. To address these issues, various research works have been done for analyzing or improving the degradation from NBTI and PBTI [6-7]. Kang et al. analyzed the impact of NBTI and PBTI on SRAM cell and concluded that the read stability degrades while write stability improves with NBTI and PBTI [6]. Lin et al. claimed that the increase in $V_{min}$ is required to ensure the functionality of SRAMs after NBTI and PBTI degradation [7]. Although the increase in $V_{min}$ is to avoid functional failure, but it is undesired in low-power applications where the energy or power consumption is a critical design constraint.

In this paper, we analyze the impact of NBTI and PBTI on the stability of 8T SRAM cells, and propose a NBTI/PBTI-aware wordline voltage control scheme. The proposed WWL voltage control technique improves the degraded stability of the half-selected cell without using boosted supply voltage and increasing the power and energy consumption.

![Fig. 1. Schematic of an 8T SRAM cell with NBTI and PBTI [8]](image)

II. IMPACT OF NBTI AND PBTI ON 8T SRAM CELL

Fig. 1 shows the schematic of an 8T SRAM cell with Q storing data ‘1’ and QB storing data ‘0’. The 8T SRAM cell consists of eight transistors, which include the conventional 6T SRAM cell, combined with the two extra stacking NMOS transistors, MR1 and MR2, as a read buffer. Unlike the conventional 6T SRAM cell, the read and write ports are separated in the 8T SRAM cell. The purpose of separating the read port from the write port is to optimize the read and write paths, respectively. However, NBTI and PBTI still exist in the cross-couple inverters as illustrated in Fig. 1. The NBTI effect occurs when the gate of a PMOS transistor is biased by data ‘0’. Similarly, PBTI exist in an NMOS transistor when the transistor’s gate is biased by data ‘1’. The NBTI and PBTI effect in an SRAM cell is unavoidable due to the positive feedback on the cross-couple inverters. In the following, we will analyze the impact of NBTI and PBTI on various SRAM cell operations. Note that all the simulation results are based on the 32nm high-k metal gate Predictive Technology Model (PTM).

This work was supported by Academic Research Fund (AcRF) Tier1, Singapore. The grant number for the project is RG 23/10 (M52040142).
A. Read Operation

In the read operation, the Read Word Line (RWL) of the selected row is turned on and the Read Bitline (RBL) is conditionally discharged depending on the stored data through the dedicated NMOS read buffer. In this case, there is no read disturbance since the storage cell is isolated from RBL. Thus, the Read Static Noise Margin (RNSM) is same as Hold Static Noise Margin (HSNM). Assuming that the read delay is defined by the time required to discharge RBL to 50% of VDD, it is obvious that the read delay is only affected by the BTI in MR1 and MR2 in Fig. 1. However, RGND is VDD and RWL is GND during non-read operation, which eliminates PBTI in MR1 and MR2. This is true regardless of the value at QB. Since MR1 and MR2 are stressed only when RWL is VDD, RGND is GND, and QB is ‘1’, the PBTI impact on MR1 and MR2 becomes negligible. Fig. 2 shows the impact of NBTI and PBTI degradation on the read delay. It verifies that the read delay is independent of the stability degradation of the storage cell.

B. Write Operation

Write operation starts by raising the Write Wordline (WWL) up to VDD to turn on the write access transistors, MA1 and MA2. One of the pre-charged write bitlines is discharged to GND to write either data ‘0’ or ‘1’ into the selected cells. When writing the opposite data, the node storing data ‘1’ is discharged through write access transistor while the node storing data ‘0’ is also charged to VDD. Once the new data is written, the positive feedback of the cross-coupled inverters quickly regenerates the new data to complete the write operation. The write ability of an SRAM cell is characterized by Write Margin (WM), which is defined as the highest write bitline voltage that can flip the stored data. Fig. 3 describes the impact of NBTI and PBTI on WM. It shows evidently that both NBTI stress and PBTI stress improve WM over time. This is because the NBTI stress weakens the PMOS transistor for maintaining data ‘1’. Similarly, the PBTI stress degrades the strength of the NMOS transistors for holding data ‘0’. Consequently, both NBTI and PBTI make data flip easier.

C. Half-Select Cell Stability

Although the read disturb has been eliminated as discussed earlier, the write disturb in the half-selected cells is still constraining the stability of the 8T SRAM cell. During write operation, all the write access transistors in the selected row are turned on by WWL. In unselected columns, write bitlines (WBL and WBLB) are floating at VDD. Thus, the half-selected cells in the unselected columns are under an unwanted disturbance condition like the conventional 6T SRAM cell. Therefore, the worst case stability of the 8T SRAM cell is still the same as the conventional 6T SRAM cell. Half-Selected Static Noise Margin (HS-SNM) is the parameter measuring the stability of the half-selected cells due to the unwanted read-like operation. It can be defined as the highest disturbing voltage at the node storing data ‘0’ that can flip the data during write operation. The BTI stress lowers the trip point of an inverter, and raises that of the other inverter, consequently degrading HS-SNM of the cell. Therefore, even if the amount of disturbance from WBL or WBLB is constant, the change in the inverters’ trip points increases the probability of data flip. Fig. 4 demonstrates the relationship between the circuit reliability (i.e. NBTI and PBTI) and the normalized cell stability. As expected, both NBTI and PBTI deteriorate the cell stability. A typical way of compensating the cell stability degradation is to raise the supply voltage at the cost of significant increase in power consumption and additional circuits for boosted supply generation. In the following section, we will present a circuit technique that can improve the stability of the half-selected SRAM cells without boosted supply voltage and performance degradation.
III. PROPOSE WORDLINE VOLTAGE CONTROL TECHNIQUE FOR IMPROVING HALF-SELECTED CELL STABILITY

In this section, we will discuss the proposed wordline (WWL) voltage control technique to improve the half-selected cell stability due to NBTI and PBTI degradation. As discussed in the last section, the stability of 8T SRAM is dominated by the HS-SNM. Once the degraded HS-SNM becomes negative, data flip will occur in the half-select cells during write operation. In order to prevent the data flip, a typical solution is to increase the supply voltage to compensate the degraded HS-SNM. However, the increase in supply voltage is undesired for low-power applications where the power or energy consumption is the utmost design constraint.

To address the above issue, in this work, we lower the WWL level to improve HS-SNM. Fig. 5 shows the relation between HS-SNM and the combined impact of NBTI and PBTI over different WWL voltages. The result shows that a lower WWL level improves HS-SNM. This is because the strength of the write access transistors is weakened with a lower WWL as its gate voltage. Hence, the disturbance current flowing from write bitlines to the cell nodes storing data '0' through the write access transistors is reduced. Write margin (WM) is another parameter also affected by the WWL voltage. Fig. 6 shows the effect of the WWL voltage on WM under ‘NBTI+PBTI’ stress. Since WM is strongly dependent upon the current strength of the write access transistors, it is apparent that WM is degraded by lowering the WWL voltage. However, the NBTI and PBTI stress improves WM over time.

This indicates that we can lower the WWL level after stress to compensate the degraded cell stability by discarding the improvement in WM by the stress. Thus, the original cell stability and the original write margin can be maintained by choosing a proper WWL voltage level.

A more comprehensive simulation result presents the relation between WM, HS-SNM, write performance, and NBTI and PBTI stress in Fig. 7. The amount of NBTI and PBTI effect over stress time is taken from the results in [1-2]. Fig. 7(a) shows the simulation result in the SRAM cell without the proposed WWL voltage control technique. It clearly shows the cell stability (HS-SNM) is decreasing as the amount of NBTI and PBTI stress time increases. Note that zero and negative HS-SNM occurs from the stress time of $10^3$. It also shows that WM and write performance is improved over the NBTI and PBTI stress. Fig. 7 (b) shows the effectiveness of the proposed WWL control scheme on the same design parameters. By employing the NBTI/PBTI-aware WWL voltage, the cell stability is improved, continuously maintaining HS-SNM above zero. In addition, WM is also maintained over the stress time even at lower WWL voltage when compared to the initial stress-free state. However, the write delay is increasing significantly from the stress time of $10^5$ onwards. Thus, it is necessary to ensure the SRAM operating frequency is able to handle the increase write delay.

**Fig. 5** The Impact of NBTI+PBTI on HS-SNM with varying WWL.

**Fig. 6** The Impact of NBTI+PBTI on Write Margin with varying WWL.

**Fig. 7** The impact of NBTI+PBTI on HS-SNM, WM, and Write Delay. The threshold voltage degradation due to PBTI+NBTI over stress time is taken from the simulation result in [9]. (a) Cell without WWL voltage control technique. (b) Cell with WWL voltage control technique.
Fig. 8 and 9 demonstrate the effect of the proposed WWL voltage control technique during write operation. Before stress, the half-selected cell has no data flip (Fig. 8 (a)). Data flip occurs with the NBTI and PBTI stress of 30mV (Fig. 8 (b)). However, the proposed technique prevents the data flip from occurring due to the improved stability with the lowered WWL voltage (Fig. 8 (c)). It can be seen that Q and QB in Fig. 8 (c) is similar to those in Fig. 8 (a) due to the disturbance reduction through the proposed technique. Note that the write operation in selected cells performs normally regardless of the stress (Fig. 9). In this work, the write speed after lowering the WWL voltage is still higher than the read speed with 256 cells per bitline. However, if the number of cells per bitline is small enough to make the write speed with lowered WWL slower than the read speed, either the amount of WWL lowering or the system clock frequency should be carefully controlled.

IV. CONCLUSION

In this paper, we have analyzed the impact of NBTI and PBTI degradation on various 8T SRAM design parameters using the 32nm high-k metal gate Predictive Technology Model. The simulation results show that the half-selected cells limit the overall SRAM stability, which is deteriorated by stress. To address the above issue, we proposed the NBTI/PBTI-aware wordline voltage control technique for improving the degraded cell stability without boosted supply voltage and significant performance degradation. We have verified that the degraded half-selected cell stability can be improved by lowering the WWL voltage without degradation in the write margin. The proposed technique can be employed by SRAMs where circuit reliability is significant.

REFERENCES