An Ultra-low Voltage, VCO-based ADC with Digital Background Calibration

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Abstract—This paper introduces an ultra-low voltage open loop VCO-based ADC with background calibration for ultra-low power applications. A novel calibration scheme is proposed to calibrate the nonlinear voltage-to-frequency tuning curve of the VCO. A replica VCO is used to compute the correction coefficients and the corrected values are stored in a lookup table. The proposed calibration method is at least 64 times faster than other state-of-the-art ones. A test chip was implemented in commercial 65nm CMOS technology. Measurement results confirm the effectiveness of the calibration scheme at 0.4 V. The proposed VCO-based ADC achieves a resolution of 8.8 bits at 10 KHz bandwidth with the power consumption of 1.15 µW in the open loop architecture.

Keywords—VCO-based ADC, Ultra-low voltage, Ultra-low power, Background Calibration

I. INTRODUCTION

With increase in applications relying on harvested energy, circuits consuming ultra-low power are being highly pursued for energy minimization. Ultra-low voltage operation is widely recommended in circuits and systems running on such strict power budgets. ADCs are fundamental parts of various sensor interface systems and have significant analog circuitry that forms a bottleneck in implementing such ultra-low voltage systems. Several Sigma-Delta (ΣΔ) architectures have been proposed for low supply voltage [1-3]. In [1], the authors discuss a Continuous Time ΣΔ modulator with passive integrators. Even though it consumes relatively lower power, the leaky integrator limits the signal-to-noise ratio (SNR) even with a higher Over-Sampling Ratio (OSR) or a higher order. This confines the use of this architecture to a finite set of applications. The driving capability of the DAC inverters and the gain of the comparator also limit the minimum operating voltage of this architecture. In [2, 3], the authors discuss higher order Discrete Time ΣΔ modulators operating at very low voltage. However, the near-threshold inverter-based amplifiers used for switched capacitor integrators suffer from low bandwidth and low gain, eventually degrading SNR. Higher order architecture is employed for improving SNR at the cost of additional current consumption.

VCO-based ADC is a promising solution to address the above problems since continuous scaling in CMOS technology aids the digital nature and the time-based architecture [4-9]. However, VCO-based ADCs need analog assistance or on-chip calibration to address the nonlinear voltage-to-frequency characteristic, which makes ultra-low voltage operation challenging. In [8], the authors discuss an ultra-low voltage bulk-controlled VCO-based Frequency Delta Sigma Modulator (FDSM) with inherent linearity by adding a header transistor offering negative feedback. However, the header transistor increases the phase noise of the VCO and thus deteriorates the SNR. The VCO power is increased in order to improve SNR, which degrades the overall Figure of Merit (FoM).

In this paper, we propose a novel calibration scheme to circumvent the distortion added by VCO. A bulk-controlled VCO-based FDSM similar to [8] is employed without header transistor. The proposed approach uses minimal analog circuitry for supply voltage scalability and ultra-low voltage operation. The proposed calibration scheme uses only 2^{15} clock cycles to compute the correction coefficients, which is 64× faster than prior arts [4, 7].

II. PROPOSED BACKGROUND VCO NONLINEARITY CALIBRATION

A sinusoidal input to a nonlinear FDSM produces a nonlinear output. The two main nonlinearities at the output are the 2\textsuperscript{nd} order and the 3\textsuperscript{rd} order harmonics. While the 2\textsuperscript{nd} order harmonics can be easily corrected using pseudo-differential architecture, the 3\textsuperscript{rd} order harmonics is difficult to measure and correct. Hence, the main objective of this work is to estimate and correct the 3\textsuperscript{rd} order harmonics. The characteristics as well as the nonlinearity of the VCO can

Fig. 1. Abstract view of the proposed VCO-based ADC architecture

-CLK

VCO-FDSM

VCO-FDSM

Signal Path

LOOKUP TABLE

D(n)

D+ D-

Dout(n)

radc + radc-

Background Calibration Block

VCO-FDSM

VCO-FDSM

Replica Path

Calibration Block

+\text{x}(t)

-\text{x}(t)

Data

Address

VCO-FDSM

VCO-FDSM

D+ D-

radc

radc+
change over time due to temperature and other variations. Therefore, background calibration is preferred since it does not interrupt the main ADC operation. The abstract view of calibration architecture is as shown in Fig. 1. Our calibration algorithm employs a replica VCO path similar to [4, 7]. Thus, the calibration algorithm is executed periodically in the replica path and the nonlinearity of the replica VCO is estimated. The signal VCO and replica-VCO are designed to be identical and hence nonlinearity in the signal path could be corrected using the estimation. Correction is done by updating a lookup table in the signal path.

Fig. 2 shows the principle of the proposed calibration for 3rd order harmonics correction. Two different sinusoids are applied to two identical nonlinear FDSMs and their outputs are added to estimate the 3rd order harmonics. The summation result contains the inter-modulation components such as $\cos(A-2B)$ and $\cos(A+2B)$, resulting from $6k_2\cos ACos^2B$, whose amplitude contains the 3rd order harmonics ($k_3$). If the inter-modulation product terms can be separated and their amplitudes are measured, the value of $k_3$ can be determined. The architecture for estimating $k_3$ utilizing the above calibration principle is illustrated in Fig. 3. $+x(t)$ and $-x(t)$ are two differential sinusoids with the frequency $f_1$ and the amplitude $A_1$. $F_d(t)$ is a square wave with the frequency $f_d$ and the amplitude $A_2$. Note that a square wave is composed of a primary frequency component and its odd harmonics. Assuming the sampling frequency is $F_S$, the frequency of $F_d/4$ is chosen for $F_d(t)$ so that the 3rd order harmonic ($3/4*F_S$) and other higher order harmonics lie outside of the Nyquist bandwidth. Since VCO-based ADCs have inherent anti-aliasing features, input frequencies higher than Nyquist bandwidth do not generate aliasing problems [5]. Thus, the square wave with the frequency of $F_d/4$ acts as a sinusoidal wave of the same frequency within the sampling spectrum. The outputs from two VCO-FDSMs (FDSM1 and FDSM2) are added as shown in Fig 3. The resultant signal is a digital signal and contains the inter-modulation product terms of $f_d + 2f_1$ and $f_d - 2f_1$. This is the same as a low frequency (2$f_1$) sinusoidal wave modulated by a high frequency ($f_d$) one. To separate the inter-modulation product terms, the output is multiplied by $f_d$ in digital domain. $f_d$ in digital domain is a square wave with the frequency of $F_d/4$ and the values of ±1. The multiplication results in a frequency shift for all the signal components. The inter-modulation product terms can be interpreted as a low frequency component with the frequency of 2$f_1$ and several higher frequency components. A 16-point moving average filter is used for removing the high frequency components and thereby smoothing the output. The amplitude of the smoothed signal is as follows

$$
\text{Calib} = 12\cdot N\cdot K_2\cdot A_1^2\cdot A_2/(\pi^2\cdot F_S)
$$

(1)

Where $N$ is the number of the VCO stages, $k_2$ is the 3rd order harmonics to be corrected, $A_1$ and $A_2$ are the amplitudes of the sinusoids, $+x(t)$ and $F_d(t)$ respectively, and $F_S$ is the sampling frequency. Since the values of $A_1$, $A_2$, $N$ and $F_S$ are known, $k_2$ can be easily calculated and is used to fill up the lookup table in the main signal path with the corrected values. The nonlinear output from the pseudo-differential FDSM, for an input $y(t)$, is as follows

$$
D(n) = \frac{2\cdot N\cdot F_S \cdot (k\cdot y(t) + k_1\cdot y(t)^3)}{\pi^2} + x\cdot D^3(n)
$$

(2)

and could be corrected by the correction coefficients as shown below

$$
D_{\text{out}}(n) = D(n) - x\cdot D^3(n)
$$

(3)

Where $D(n)$ is the uncorrected value, $D_{\text{out}}(n)$ is the corrected value and 'x' is the correction coefficient. Using (1), (2) and (3), the correction coefficient 'x' could be found.

$$
x = \frac{\text{Calib} \cdot \pi^2}{[6\cdot A_1^2\cdot A_2]}
$$

(4)

III. IMPLEMENTATION OF THE PROPOSED ADC

A. VCO-FDSM

Fig. 4 shows the block diagram of the proposed VCO-FDSM. For simplicity, only a half of the pseudo-differential FDSM (PD-FDSM) is illustrated with key blocks. VCO consists of 16 stages of VCO delay cells. Each VCO delay cell is implemented using a differential CMOS inverter with PMOS whose bulk is controlled by the input signal. The output of the VCO delay cells are buffered and sampled using sense amplifier flip-flops (Φ-Sampler). The 16-stage VCO has 32 distinctive phase states. The sampled phase is encoded by a standard 32:5 state encoder (Φ-Encoder). After that, the digital differentiator calculates the number of state changes between the present state and the previous state. The number of state changes in one clock cycle is the digital equivalent of the analog input. Two identical VCO-FDSMs with two opposite phase inputs are employed in pseudo-differential fashion. The outputs from the PD-FDSMs are subtracted to get 6-bit output.
B. Proposed Calibration Implementation

Fig. 5 shows the internal architecture of the proposed calibration scheme. The analog generation block generates $\pm x(t)$ and $F_d(t)$ to compute the nonlinearity coefficients as discussed in section II. It is designed by 2rd order RC low pass filters. The sinusoidal $\pm x(t)$ is created by this block using a square wave with the frequency of CLK/128, i.e. 10KHz. Hence, the low pass filter has the cut-off frequency of 10 KHz. The generated sinusoids $\pm x(t)$, $\pm F_d(t)$ and $\pm x(t)+F_d(t)$ are applied to the replica VCO-FDSM whose output is passed on to the peak detectors to estimate $A_1$, $A_2$ and $Calib$ described in (4). The coefficient calculation block finds the correction coefficient using the peak detector outputs. The correction coefficient is then used to find the corrected values using (3). Lookup table is filled with 15 bit corrected value using 6-bit uncorrected value as the address. The proposed calibration sequence is indicated in Fig. 6. It takes approximately $2^{15}$ clock cycles for one entire calibration cycle, which is much faster than other state-of-the-art calibration techniques.

The VCO-FDSM and the analog generators were implemented using custom circuits; digital blocks in the calibration scheme such as the peak detector, the coefficient-calculation block and the lookup table were implemented using Verilog-HDL and synthesized using standard cell libraries. Therefore, the proposed calibration technique can be easily transferred to other CMOS technologies.

IV. MEASUREMENT RESULTS

The proposed calibration algorithm was implemented in 65nm technology so that its effectiveness in ultra-low voltage operation could be verified. Since our target specification for bandwidth is 10 KHz, we use a sampling frequency of 1.28MHz and OSR 64. Correction coefficient found on chip was used to fill in the lookup table. Fig. 7 shows the $2^{15}$-point FFT plots of output before and after calibration for an input sinusoid of frequency little higher than 1.8 KHz and amplitude 300mVpp. Even order distortions dominate the corrected output, due to layout mismatch. As it can be seen from the Fig. 7 SNDR improved by more than 13dB from 42dB to 55dB. Fig. 8 shows the plot of measured SNDR for different input amplitudes with and without calibration. Fig. 9 shows the die photograph of the chip. The design occupies a total area of 0.24mm$^2$. The signal VCO FDSM and replica VCO FDSM together consume 2.3$\mu$W, the analog waveform generator consumes 0.3$\mu$W and the Background Calibration consumes 2$\mu$W. It takes only 5ms to run one calibration cycle, hence the
calibration block including replica VCO could be disabled intermittently. Thus, the total power consumed by the ADC is only 1.15µW. Table -1 compares this work with state of the art designs.

V. CONCLUSION

VCO-based ADCs are promising candidates for achieving ultra-low power consumption at ultra-low voltages. We have proposed a novel calibration algorithm suitable for non-linearity correction in VCO based ADCs with ultra-low voltage supplies. Proposed calibration algorithm is the fastest among existing algorithms. The effectiveness of the calibration scheme is validated by a functioning prototype at 0.4V. The SNDR and SFDR improved considerably after the calibration cycle. Figure of Merit (FoM) is comparable to the state of the art designs. The resolution is limited by the phase noise of the VCO. Careful design of VCO for lower phase noise can yield better resolution. Currently, the operating voltage is limited by the use of logic cells from standard cell libraries. Design could operate at lower supply voltages with the use of custom designed standard cell libraries.

Table 1. Comparison with state of the art designs

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REFERENCES


