A 76% Efficiency Boost Converter with 220mV Self-Startup and 2nW Quiescent Power for High Resistance Thermo-Electric Energy Harvesting

Abhik Das1, 2, Yuan Gao2, Tony Tae-Hyoung Kim1
1Nanyang Technological University, Singapore, 2Institute of Microelectronics, Singapore
Abhik2@e.ntu.edu.sg

Abstract—With the emergence of thin-film thermo-electric generators (TEG), power density and sustainability of energy harvesting sources have improved. These novel power sources however exhibit high internal electrical resistances. Conventional state-of-the-art boost converters encounter low efficiency and potential startup failures when harvesting energy from such sources. This paper presents a highly efficient boost converter for thermo-electric energy harvesting systems based on a novel Power-on-Reset (PoR) driven startup circuit. It utilizes the feedback between TEG, the boost converter, and the PoR circuit, converting a reset signal edge into a train of pulses. The proposed startup circuit is automatically disabled once startup operation is completed, and consumes the quiescent power of 2nW in steady-state. The proposed boost converter has a self-startup TEG voltage of 220mV and a peak power conversion efficiency of 76% with a minimum input for operation being 85mV.

I. INTRODUCTION

Thermal energy is one of the most ubiquitous sources, desirable for implantable and wearable devices. Various renewable energy harvesters powered from light, vibration, thermal, or bio-fuel sources are available depending on system power dissipation, physical size, and reliability [1-2]. Such energy sources replace batteries, provide long-lasting operation for sub-mW applications, and eliminate the difficulty in recharging and replacing it. Thermo-electric generators (TEG) can manifest as temperature difference ($\Delta T$) under any environmental conditions, making it more desirable. Improved TEG elements such as MPG-D751 which uses compounds of Bi, Sb, Te and Se, achieve smaller device area with increased power density (100W/mm²), compared to conventional bulk-material-based TEGs (2W/mm²) at $\Delta T$ of less than 10 °C, which enables system miniaturization.

Electrically, a TEG can be modelled as an ideal voltage source in series with internal resistance ($E_{SR}$). The physical dimensions of a TEG and the temperature difference between human body and ambient are limited. Therefore, battery-less startup from low voltages and power is challenging. One of the major factors limiting the electrical startup is the threshold voltage of MOSFETs. Advanced CMOS technology can overcome this limitation at the cost of higher leakage power. As an alternative solution, a startup circuit with the startup voltage of 35 mV is reported [3]. However, it uses a MEMS switch to aid the turn-on action at ultra-low voltage. The limited available power and voltage makes battery-less self-startup even more difficult, affecting the operations of the previously reported circuits [3-10]. In this paper, we propose a PoR-based startup circuit with self-control of the duration and frequency of the PoR pulses during startup. The pulses are initiated due to the
difference in the voltage drops across the $E_{SR}$ at different circuit conditions. The proposed startup circuit is automatically disabled after startup to minimize the power and leakage.

II. PROPOSED HARVESTER ARCHITECTURE AND OPERATIONS

The proposed energy harvesting system is illustrated in Fig. 1. It consists of four main blocks; namely, Boost Converter Core (BCC), Starter, Pulse Generator for Steady-state (PGS) and Decision Switch (DS). DS and PGS form the Control Unit for steady-state operation. The Starter consists of Power-on-Reset (PoR) and Charge Pump (CP). BCC has two sub-blocks, Auxiliary Booster (AB) and Main Booster (MB). The AB block is comprised of a NMOS (M1), a diode-connected PMOS (M3), an inductor (L1) and a capacitor (COUT). Although conventional PoR does not produce oscillating waveforms, the proposed PoR block automatically generates a chain of pulses based on feedback action and the available finite $E_{SR}$ of TEG at the falling edge before resetting completely. The PoR-generated CLK1 drives CP and M1. The peak amplitude of CLK1 at low voltages is lesser than M1’s threshold voltage. CLK1 is therefore used to boost VIN to a higher voltage CPOUT (Fig. 2) using CP, which powers PGS and MB (M2 replaces M1 to form MB) in CP mode to boost VOUT (when $VOUT < 0.45V$). The schematics of AB and MB are depicted in Fig. 3 (a) and 3 (b), respectively. If the CP mode still persists after CLK1 settling at 0V, VOUT will be eventually discharged. To avoid this, once VOUT is charged to a preset voltage of 0.45 V, DS will switch the power supply of PGS from CPOUT to VOUT for normal operation (VOUT mode).

PoR is a reset circuit that is incorporated to detect power applied to a chip and generate a reset impulse response for the chip. The proposed PoR (Fig. 4) is designed to improvise the ideal characteristics observed in PoR discussed in [10]. At the beginning of startup, all the nodes inside the PoR circuit are at 0 V. VIN charges the on-chip capacitor C1 through the transistors P4 and N4. Before the node D is charged beyond the switching threshold of INV1 (ST_INV), Y follows VDD and the node X remains LOW. M1’s gate driven by CLK1 has the same polarity as Y and follows VDD. With the rise of VDD, M1 is turned on weakly and the conduction current I1 (Fig. 5(a)) charges L1. When D is rises beyond ST_INV, Y starts falling and M1 is turned off. The decrease of conduction current (I2 in Fig. 5(b)) leads to smaller voltage drop across r. This increases the VIN level, which increases the ST of the inverters in PoR. If the voltage level at D (VD) is still lower than the instantaneous ST_INV, CLK1 becomes HIGH again. Therefore, the action of Y propagating to CLK1, which varies the voltage drop across r, results in an oscillating nature of CLK1 (Fig. 6), and continues until VD becomes greater than ST_INV during the off-state of M1. This disables Starter and M1 that minimizes the quiescent power in both. The frequency of CLK1 is proportional to VIN and the size of N1, and inversely proportional to r. The pulse duration and the number of pulses increase with VIN and r. While they decrease with...
N, C1 affects only the start-time.

During phase (a), M1 is weakly conductive operating in the sub-threshold region where Vx drops to enable the conduction current (I1) during this short interval. Because of the inductor’s nature to resist a change across it, Vx will rise again. At this point, as explained in phase (b), M1 reaches sub-threshold saturation condition, and the current through L stops rising and decreases with a small slope (VCLK >4UT). When CLK1 becomes ‘0’, the current though M1 is cut-off, forcing Vx to shoot sharply and turn M3 on, during which L discharges all its charges to COUT. UT is the thermal voltage.

Dickson’s CP and the measured COUT waveform are shown in Fig. 7 and Fig. 8, respectively. Note that COUT will eventually decay if no switching from the CP mode to the VOUT mode occurs during steady-state due to the absence of pulses in CLK1. Therefore, the system switches its control from the CP mode to the VOUT mode during this instant. Selection between the CP mode and the VOUT mode is made by DS (Fig. 9). DS comprises a multiplexer (MUX) and a detector (DET). When the DET output (X) is at 0 (until VOUT<450mV), MUX selects the CP mode. When VOUT>450mV, the VOUT mode is selected by MUX. After this, X1 follows VOUT. PGS consists of a controlled ring oscillator (Fig. 10) followed by a frequency divider and a gate buffer for driving M2 with the clock CLK2 in steady-state (VOUT mode).

III. MEASUREMENT RESULTS

The proposed harvester system is implemented in a 65-nm CMOS process. The harvester module contains TE-CORE7 [11] which contains the standalone Thermo-Generator Package, TGP-751. For simplified measurements, a controlled power supply with a series resistor (r) is used to emulate the target TEG. For characterization and measurements of MPG-D751 with the designed circuit, the power management circuit inside the module was disconnected from MPG-D751. MPG-D751 exhibits an electrical resistance of between 240 - 350Ω. The characteristics of Micropelt’s TEG (MPG-D751) is shown in Fig. 11. Characterization and measurements of the proposed harvester with TEG has been executed after disabling the module’s boost converter.

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The startup operation at VTEG of 220 mV and r = 350Ω is demonstrated in Fig. 12 (a). The exploded view of CLK1 pulses is highlighted in Fig. 12 (b). The resetting of CLK1 and accordingly the Starter enhances the voltage gain further. The PoR pulses reset after a finite period and VOUT settles at 1.3 V. As shown in Fig. 13, at r = 70Ω, the minimum startup voltage of 170 mV was obtained. At lower values of r (0-70Ω), the startup voltage is inversely proportional to r. At higher values of r (70 - 450Ω), however, the higher voltage drop reduces the available VIN. After startup operation is completed, it can harvest energy from the minimum voltage of 85 mV boosting VOUT to 550 mV. VOUT settles where the power loss in HS is equal the harvested power. The peak efficiency at r = 350Ω is 76% at the input of 180 mV as shown in Fig. 14. The quiescent power of Starter and M1 together is 4nW, is 0.4% of the input power at 90 mV. The quiescent power and the efficiency are measured at VTEG of 220 mV and the input resistance of 350Ω after the circuit has acquired steady-state. At VIN > 550 mV, the increased leakage in M1 and Starter degrades the quiescent power.

**Table I: Comparison chart with state-of-the-art work**

<table>
<thead>
<tr>
<th>Min. VTEG (mV)</th>
<th>Start-up volt. (mV)</th>
<th>Peak Eff. (%)</th>
<th>Process (nm)</th>
<th>Start-up mech.</th>
<th>QP (%)</th>
<th>Min. VIN (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>150</td>
<td>330</td>
<td>61</td>
<td>450</td>
<td>Trr†††</td>
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<td>85</td>
</tr>
<tr>
<td>170</td>
<td>350</td>
<td>85</td>
<td>220</td>
<td>PoR</td>
<td>40</td>
<td>40</td>
</tr>
<tr>
<td>190</td>
<td>380</td>
<td>76††</td>
<td>180</td>
<td>PoR</td>
<td>40</td>
<td>40</td>
</tr>
<tr>
<td>210</td>
<td>220 (170)*</td>
<td>76††</td>
<td>180†</td>
<td>PoR</td>
<td>40</td>
<td>40</td>
</tr>
<tr>
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<td>220 (170)*</td>
<td>76††</td>
<td>180†</td>
<td>PoR</td>
<td>40</td>
<td>40</td>
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<tr>
<td>250</td>
<td>220 (170)*</td>
<td>76††</td>
<td>180†</td>
<td>PoR</td>
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**REFERENCES**


