A 457-nW Cognitive Multi-Functional ECG Processor
Xin Liu1, Jun Zhou1, Yongkui Yang1,2, Bo Wang1,2, Jingjing Lan1, Chao Wang1, Jianwen Luo1, Wang Ling Goh2, Tony Tae-Hyoung Kim2, and Minkyu Je3
1Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), Singapore
2School of EEE, Nanyang Technology University, Singapore
liux@ime.a-star.edu.sg, zhouj@ime.a-star.edu.sg

Abstract— In this paper, a multi-functional ECG signal processor for wearable and implantable real-time monitoring is presented. To enable extremely long-term ambulatory monitoring, several power saving techniques are proposed, including global cognitive clocking, pseudo-downsampling wavelet transform, adaptive storing, and denoising-based run-length compression. An on-chip low-complexity cardiac signal analysis module is proposed to realize comprehensive analysis functions. Near-threshold circuit technique is applied to the overall system. Implemented in 0.18 μm CMOS, the proposed cognitive ECG processor consumes only 457 nW at 0.5 V supply for real-time ambulatory monitoring. Compared with existing designs, the presented ECG processor achieves the lowest power consumption.

Keywords—ECG, processor, wavelet transform, low power

I. INTRODUCTION

Long-term ambulatory ECG is highly desired to detect, characterize, analyze, and document for cardiac disease diagnosis and management in clinical practice. Hence several ECG processors have been developed [1]–[5]. The ECG processor design for long-term monitoring is challenging because the power consumption should be extremely low to maximize the lifetime of its power source. Some processors have an embedded RISC core to realize reconfigurability on diverse functions [1], [2]. However, the power consumption is relatively high. Several application-specific ECG processors without RISC core have been reported with lower power consumption [3]–[5]. Most of them mainly focus on QRS detection. However, for advanced ECG monitoring, more comprehensive cardiac analysis functions are required [6], [7]. Since increased complexity of processing algorithms significantly increase power and silicon area consumption, on-chip implementation of advanced analysis functions are not straightforward.

In this paper, we propose a real-time multi-functional ECG processor. To achieve ultra-low power consumption, various power-saving techniques are applied from architecture to circuit level. Cognitive clocking technique is applied to the overall system which can switch between different clock frequencies automatically based on different temporal resolution requirements. An ultra-low-voltage ADC is implemented using adaptive clocking. As a large number of storage units consume significant power and area, several processing schemes are developed to reduce the number of storage units and maintain satisfying performance. Such schemes include pseudo-downsampling wavelet and inverse wavelet transforms, adaptive storing, and denoising-based run-length compression. Similar to [3], noise and interference suppression are performed to reconstruct the clean ECG waveform. To enable comprehensive on-chip cardiac analysis, a low-complexity reconfigurable signal processing module is designed. It can realize P/QRS/T detection, morphology identification, as well as PR/RT/RP interval calculation. With all these design techniques applied, the proposed ECG processor achieves extremely low power consumption, making it well suited for power-constrained long-term ambulatory cardiac monitoring.

II. COGNITIVE MULTI-FUNCTIONAL ECG PROCESSOR

A. System Architecture

The system block diagram of the proposed ECG processor is shown in Fig. 1. An ultra-low-voltage digital-assisted adaptive SAR ADC is implemented to digitize the acquired analog ECG signals. A digital signal processing engine (DSPE) performs noise/interference suppression, cardiac signal analysis, and clean ECG reconstruction, based on quadratic spline wavelet transform (WT) & inverse WT (IWT) [6]. Considering ECG signal characteristics and for achieving comparatively higher temporal resolution, the maximum sampling rate of the ECG signal is 500 Hz in our system, and thus 4 scales of WT is sufficient to perform the required signal processing. There are 4 types of WT filters: decomposition high-pass filter...
(DHPF), decomposition low-pass filter (DLPF), reconstruction high-pass filter (HRPF), and reconstruction low-pass filter (RLPF). A cardiac signal analysis module performs P/QRS/T detection and analysis using DHPF outputs. To achieve significant power reduction, the overall system operates at adaptive clock frequencies depending on the required temporal resolutions. A cognitive clock manager tracks the input signal characteristic and generates adaptive operation clocks accordingly for different modules. Key design efforts are described in details in the following subsections.

B. Global Cognitive Clocking Scheme

In the morphology of ECG waveform, the most significant characteristics are P wave, QRS complex, and T wave. The QRS complex’s analysis requires higher sampling rate with low duty cycle (~ 23%), whereas P and T waves’ analysis require lower sampling rate with higher duty cycle. According to [6] and [7], the main energy of QRS and P/T are at 8 – 27 Hz and 4 – 13.5 Hz, respectively. Therefore, to maximize the efficiency, instead of constant operation clocking, we propose cognitive clocking scheme for the overall system. As shown in Fig. 1, DHPF output on Scale 2 (DHPF_S2) is compared with a cognitive clock, and ADC output are shown in Fig. 2. This ultra-low-power consumption. The measured ADC input, adaptive sampling plate sampling technique are utilized to minimize power consumption.

C. Ultra-Low Voltage ADC with Adaptive Clocking

A 0.5 V 8.1-ENOB non-binary redundant SAR ADC is implemented with adaptive clocking as shown in Fig. 2. The ADC internal clock frequency $f_{ADC}$ and sampling clock frequency $f_{samp}$ can switch between fast (6 kHz/500 Hz) and slow (3 kHz/250 Hz) frequencies using the glitch-free multiplexer in the cognitive clock manager. A bootstrapped switch with gate signal swing from 0 to 2VDD is used to reduce switch delay and improve linearity of the sampling circuit while operating at ultra-low voltage. Single-ended structure and top-plate sampling technique are utilized to minimize power consumption.

D. On-Chip Cardiac Signal Analysis

The system can perform basic ECG analysis functions such as noise/interference suppression and QRS detection. In addition, more comprehensive cardiac analysis functions can be realized using the proposed low-complexity cognitive signal processing scheme, including P/T peak detection, P/QRS/T wave morphology identification, and PR/RT/TP interval calculation. The morphologies that can be detected include positive (+), negative (−), biphasic (+/− or −/+), only upwards (OU), and only downwards (OD). Taking advantage of the fact that P, QRS, and T occur sequentially and the analysis procedures are similar, we propose a sequential processing flow as shown in Fig. 3. There are two levels of

<table>
<thead>
<tr>
<th>3dB Bandwidth (Hz) of WT Scales</th>
<th>[4]</th>
<th>[6]</th>
<th>[7]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{samp}$</td>
<td>300</td>
<td>250</td>
<td>250</td>
<td>500</td>
</tr>
<tr>
<td>S1</td>
<td>75-150</td>
<td>62.5-125</td>
<td>62.5-125</td>
<td>125-250</td>
</tr>
<tr>
<td>S2</td>
<td>21.6-70.2</td>
<td>18.5-58.5</td>
<td>18.5-58.5</td>
<td>62.5-125</td>
</tr>
<tr>
<td>S3</td>
<td>9.6-32.4</td>
<td>8-27</td>
<td>8-27</td>
<td>18.5-58.5</td>
</tr>
<tr>
<td>S4</td>
<td>4.8-16.2</td>
<td>4-13.5</td>
<td>4-13.5</td>
<td>8-27</td>
</tr>
<tr>
<td>QRS</td>
<td>S3</td>
<td>S1-S4</td>
<td>S1-S4</td>
<td>S4</td>
</tr>
<tr>
<td>P/T</td>
<td>--</td>
<td>S4</td>
<td>S4</td>
<td>--</td>
</tr>
</tbody>
</table>

Figure 2. Proposed ultra-low voltage ADC design with adaptive sampling.
state transition. The top-level state transition controls the processing behavior switching between $P,QRS$, and $T$ searching periods. DHPF_S2 is used to control the top-level state transitions. During $QRS$ searching period, the system uses high operation frequency, while the low operation frequency is used elsewhere. The second-level state transition controls the detailed signal analysis flow under each searching period, as shown in Fig. 3. DHPF_S4 is used as input signal, and it should be emphasized that the actual signal components used for $P/T$ searching and $QRS$ searching are different, as shown in Table I. The state transitions under each searching period can be represented by 9 stages at most. The transaction behaviors in different periods are similar, but different parameter configurations are used. Therefore, for different searching periods, the detailed cardiac analysis can be reconfigured and most of the hardware resource can be shared. Furthermore, there is no need to switch the input signal for different searching periods. Pipeline structure is also adopted so that the highest required operation frequency for cardiac signal analysis is the same as the input sampling rate.

E. Pseudo-Downsampling WT & IWT and Adaptive Storing

Non-downsampling WT is adopted for ECG signal analysis because of time invariance and satisfying temporal resolution [6, 7]. However, it introduces a huge number of storage units in WT and IWT modules during FIR filtering [3]. To reduce the number of storage units, we propose pseudo-downsampling WT and IWT (PDWT and PDIWT), as shown in Fig. 4(a). The average increment $\Delta y_j(k)$ between WT outputs $y_j(k*2^n)$ and $y_j((k+1)*2^n)$ is calculated and stored. We store DHPF and DLPF outputs in every $2^m$-1 samples, i.e. $y_j(k*2^n)$, where $k=0,1,2,\ldots$. For $y_j(k*2^n)$ between $y_j(k*2^{n+1})$ and $y_j((k+1)*2^{n+1})$, we compare it with a threshold $T_0$, which is calculated based on $y_j(k*2^n)$ and $\Delta y_j(k)$. If $y_j(k*2^n)$ exceeds $T_0$, then it is a significant wavelet output, and its actual value is saved in the storage units. Otherwise, we just linearly approximate the value of $y_j(k*2^n)$ using $y_j(k*2^{n+1})$ and $\Delta y_j(k)$, so that its actual value does not need to be saved. In Fig. 4(b), for example, WT Scale 4 outputs $y_4(2)$ and $y_4(6)$ are the significant wavelet outputs, and thus $y_4(0)$, $y_4(2)$, $y_4(6)$, $y_4(8)$ and $\Delta y_4(0)$ need to be saved. Using this method, the number of required storage units can be greatly reduced while maintaining the significant wavelet outputs, resulting in great power reduction without much performance degradation. Since DLPF and DHPF outputs of higher scales correspond to lower-frequency signal components, the number of significant wavelet outputs tends to be small, and thus the required number of additional storage units for them is comparatively low.

F. Denoising-Based Run-Length Compression

Another place where a huge number of storage units are consumed is the synchronization delay module between WT and IWT, especially for lower scales [3]. In our DSPE, the threshold-based zero-forcing denoising scheme is adopted on low scales. After denoising, DHPF outputs of low scales are dominated by zeros and only small portion contains continuous non-zero values, as shown in Fig. 1. Inspired from this fact, the denoising-based run-length data compression (DBRLC) scheme is proposed. As shown in Fig. 1, the non-zero data will be stored in the storage units. Once continuous zeros are detected, a flag will be written into storage units. Following that, the counted number of zeros is written into storage units, followed by the next non-zero data. At the input of PDIWT, once the flag of ‘0’ is detected, a certain number of continuous ‘0’ will be fed into PDIWT. By this DBRLC, the required number of storage units for synchronization delays is significantly reduced without signal distortion. Benefiting from the reduced number of storage units, the power and area consumption of the overall system is further reduced.

III. CHIP IMPLEMENTATION & MEASUREMENT RESULTS

The proposed ECG processor has been fabricated using 0.18 $\mu$m CMOS process because of its relatively low leakage and process variation which are especially beneficial for near-threshold operation applications. The supply voltage of the ECG processor can be scaled down to 0.5 V. The chip micrograph and specification summary are provided in Fig. 5. Comparison between the presented design and other existing designs is made in Table II. The proposed ECG processor can realize comprehensive cardiac analysis functions. At the same
time, it outperforms other designs in terms of power consumption, making this design very well suited for wearable and implantable long-term monitoring where the power budget is extremely critical. The presented ECG processor consumes only 457 nW including both ADC and DSPE. In Fig. 6, the power reduction breakdown is presented. The total power consumption can be reduced by 63% using the proposed architectural-level power-saving techniques (i.e. global cognitive clocking, PDWT & PDIWT, adaptive storing, and DBRLC), compared to the conventional design. Combined with near-threshold circuit design technique, a total power reduction of 96% can be achieved.

Measurement results using a logic analyzer are shown in Fig. 7. The input ECG signal is distorted by noise. It can be observed that the clean ECG is reconstructed after noise/interference suppression. The reconstructed ECG using \( f_{\text{DSP}} \) is also presented, in which some distortion can be observed. It is the reason why the output buffer with \( f_{\text{DSP}} \) is used to avoid distortion of the reconstructed ECG caused by the dynamic operation frequency. \( P/QRS/T \) identification and morphology detection can be correctly obtained (i.e. index_\text{P}, index_\text{QRS}, index_\text{T}). The detection performance in terms of sensitivity (Se) based on MIT-BIH database is presented in Fig. 7, which is fairly good considering the low complexity and low power consumption achieved. In the future, we will further improve the detection performance of the proposed on-chip cardiac signal analysis scheme.

IV. CONCLUSIONS

A cognitive multi-functional ECG processor has been designed and fabricated in 0.18 μm CMOS process. Various power-saving techniques are applied across different levels of design hierarchy, including global cognitive clocking, pseudo-downsampling WT & IWT, adaptive storing, denoising-based run-length compression, and near-threshold operation. The presented processor realizes comprehensive cardiac analysis functions while consuming only 457 nW from 0.5 V supply voltage, which is the lowest consumption among the processor designs for long-term ECG monitoring.

REFERENCES


TABLE II. COMPARISON WITH THE EXISTING ECG PROCESSORS

<table>
<thead>
<tr>
<th></th>
<th>This Work</th>
<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
<th>[5]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process (µm)</td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
<td>0.35</td>
<td>0.18</td>
</tr>
<tr>
<td>Max Freq. (Hz)</td>
<td>3k/6k (ADC) 250/500 (DSPE)</td>
<td>250-1k</td>
<td>1k</td>
<td>300</td>
<td>1M</td>
</tr>
<tr>
<td>Voltage (V)</td>
<td>0.5</td>
<td>1.8</td>
<td>1</td>
<td>1.8</td>
<td>1.8</td>
</tr>
<tr>
<td>Functions*</td>
<td>1-5</td>
<td>1-3, 6</td>
<td>1-3, 6</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Power (µW)</td>
<td>0.022 (ADC) 0.435 (DSPE)</td>
<td>6</td>
<td>29</td>
<td>0.83</td>
<td>176</td>
</tr>
</tbody>
</table>

*Functions: (1) Noise/interference suppression; (2) QRS Detection; (3) Clean ECG reconstruction; (4) P/T detection; (5) P/QRS/T morphology detection; (6) Encryption

Figure 5. Chip micrograph and specification summary.

Figure 6. Power reduction breakdown using proposed techniques.

Figure 7. Measurement results of the proposed cognitive ECG processor.