A 0.6-V Power Efficient Digital LDO with 99.7% Current Efficiency Utilizing Load Current Aware Clock Modulation for Fast Transient Response

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Abstract—This paper describes a fully integrated, low voltage digital low-dropout voltage (DLDO) regulator for ultra-low power applications with a load current aware clock modulation scheme. The proposed DLDO uses a clock modulation technique that provides a fast transient response during load state transitions. The proposed clock modulation (CM) controls the clock frequency when it senses a sudden load current transition. This eliminates the tradeoff between transient time and power efficiency with a fixed clock frequency. Thus, it minimizes the transient response time and maximizes the power and current efficiency. The proposed DLDO operates at 0.6 V and generates 0.55 V output voltage. A test chip is fabricated using 65-nm CMOS technology and demonstrates the current efficiency of 99.7% with the load current from 10 µA to 200 µA with and the quiescent current of 0.9 µA.

Keywords—Digital low dropout; current efficiency; linear regulator; load response; power management.

I. INTRODUCTION

Recent progress in integrated circuit (IC) technology and design techniques, especially in the ultra-low power circuit domain, has led the appearance of fully integrated autonomous and implantable systems-on-chip (SoC) by the scaling down of supply voltage to near/sub-threshold region (i.e. < 0.5) [1, 2]. Many applications such as biomedical devices and wireless sensor nodes in IoT systems have taken advantages of such a progress. As the supply voltage scales down, IoT systems and medical sensors circuits can be totally integrated in a chip with ultra-low power consumption. To meet this low power consumption requirement, low power and efficient LDOs need to be designed. Analog LDOs have been a very strong candidate in linear regulator power management circuits for various SoC applications [3, 4]. However, analog LDOs have poor performance at low supply voltage due to high quiescent current [5]. For these reasons, digitally controlled LDOs have attracted researchers’ attention.

Several digital LDO (DLDO) works have been reported in literature. In [2], a DLDO with low quiescent current and supply voltage of 0.5 V is proposed for low power applications. However, low power consumption was achieved at the cost of slower transient response. The design was improved in [6] by introducing an analog LDO in parallel with the DLDO in [2]. This increased the quiescent power drastically. The work in [7] describes a reconfigurable DLDO for fast transient response to cover a wide load range. However, it targets maximum current of 4.6 mA with increased quiescent current, which is suitable for our target applications (e.g. biomedical, IoT and energy harvesting applications). In [8], a fast transient response DLDO is proposed at the supply voltage of 1.39 V. A low voltage DLDO with 0.39 V is proposed in [1]. However, the proposed control technique needs a VCO and assumes digitally converted reference voltage, which implies the design of an analog-to-digital converter.

All the research works mentioned above concentrates either on low power or fast transient for load regulation. This work addresses the gap between the speed and the power of LDOs. This work proposes a clock modulation technique for achieving low power consumption and fast transient response with varying load.

II. PROPOSED DLDO

A. Conventional DLDO

A conventional DLDO structure is illustrated in Fig. 1. It consists of a comparator, delay elements, a digital controller and a PMOS array as power switches. The comparator compares \( V_{\text{out}} \) with \( V_{\text{ref}} \), and the digital controller uses the comparator output for controlling the PMOS array through a serial-in-parallel-out bi-directional shift register. The comparator detects the drop/overshoot at \( V_{\text{out}} \) and signals the shift register to turn ON/OFF the power switches. The shift register controls the number of ON switches depending on the comparator decision. Each switch is turned ON/OFF with the system clock. Therefore, the output voltage regulation is
dependent on the clock frequency. If the clock frequency is high, the output voltage transient response time decreases. However, this degrades the overall efficiency and increases the quiescent current. This requires a tradeoff between the output transition response time and the efficiency, which is the main focus of this work.

B. Proposed DLDO Architecture

In order to address the tradeoff issue of the conventional DLDO, this work proposes a DLDO with clock modulation (CM). The proposed DLDO architecture is depicted in Fig. 2. The proposed CM senses load transition states, and switches the clock to higher frequency when the load current changes dramatically. This allows \( V_{\text{out}} \) to track \( V_{\text{ref}} \) with small response time. Once \( V_{\text{out}} \) becomes close to \( V_{\text{ref}} \), the CM block put the clock frequency for the shift register to the normal lower frequency to decrease the power consumption during the constant load state and hence increase the efficiency. The proposed CM block detects both substantial increase and substantial decrease in the load current. In this work, 8MHz and 1MHz are used as higher frequency and lower frequency for controlling the shift register with 64 PMOS switches. This covers the load current from 10 \( \mu \)A to 200 \( \mu \)A. The detailed operation of the proposed CM is explained in the following section.

C. Clock Modulation for Fast Transient Response

Fig. 3 illustrates the proposed CM block. It consists of a peak detector (PD) and a valley detector (VD) to detect the load current transition from low to high and high to low, respectively. At steady state condition, the DLDO output voltage has small ripples due to the continuous switching of the PMOS switches by the controller. When a large load transition from low to high occurs, \( V_{\text{out}} \) stays below \( V_{\text{ref}} \) for a longer time. It also depends on the decoupling capacitor size. If the decoupling capacitor is too big, it takes a more number of clock cycles for \( V_{\text{out}} \) to follow \( V_{\text{ref}} \). A higher clock frequency is utilized through the proposed CM block when this situation happens. In this work, the higher clock frequency is activated when the comparator output generates ‘1’ or ‘0’ continuously over the five clock cycles. This is detected by the peak detector (PD) and the valley detector (VD) depicted in Fig. 4 and Fig. 5. The number of DFFs can be easily controlled based upon the target system requirements. The PD consists of five DFFs connected in series as shown in Fig.4. The outputs of the DFFs are connected to \( V_{\text{dd}} \) through the PMOS set control. Similarly the VD has five series DFFs as described in Fig. 5. The outputs of them are tied to \( V_{\text{ss}} \) through the NMOS reset switch.

Fig. 6 shows the timing diagram explaining the operation concept of the proposed CM scheme. Initially, the outputs of the VD and PD are set to ‘1’ and ‘2’, respectively. The outputs of both detectors are XOR-ed, which produces ‘1’ a default condition at the XOR output (Fig. 3). As shown in Fig. 3, the XOR output is sent to the clock selector (MUX) which selects either lower clock frequency (1MHz) or higher clock frequency (8MHz). Since the XOR output is initially ‘1’, the slower clock (i.e. 1MHz) is selected and supplied to the controller. When the load current increases significantly, \( V_{\text{out}} \) drops below \( V_{\text{ref}} \) and the comparator output becomes ‘0’. The controller increases the number of on power transistors at each clock cycle (1MHz). At the first rising edge of the clock to the detectors, ‘0’ signal is passed to ‘Q0’ of the 1st DFF of both
detectors as shown in Fig. 4 and Fig. 5. For the VD, since all PMOS control is connected to $Q_{\overline{BA}}$, which is ‘1’, all the switches are turned OFF making ‘0’ from comparator to traverse with clock edges. After four consecutive clock rising edges, ‘0’ is transferred to last DFF in the series. On the contrary, in PD, ‘0’ from the comparator turns ON the NMOS control switches and hence all the outputs of the DFFs are pulled down to ‘0’. After four clock rising edges which is considered load transition detection time for the proposed CM scheme, XOR is triggered to ‘1’ indicating a load transition. Hence, the MUX output is switched from low to high frequency clock. Once $V_{\text{out}}$ crosses $V_{\text{ref}}$ using the higher clock frequency, the PD and VD will be restored to their default condition and the controller is supplied with low frequency clock (i.e. 1MHz) which reduces the power consumption tremendously at steady state.

III. MEASUREMENT RESULTS

The proposed DLDO with CM is implemented in 65nm CMOS process with the area of 0.037 mm². Fig. 7 shows the test chip microphotography. It operates at 0.6 V with 50 mV dropout voltage covering load range from 10 μA to 200 μA. Fig. 8 explains the current efficiencies across the load range. The proposed DLDO achieves a maximum current efficiency of 99.7% at 200 μA current load, with 0.9 μA quiescent current. Fig. 9 shows the transient $V_{\text{out}}$ waveform when $V_{\text{ref}}$ and $V_{\text{dd}}$ changes from 0 V to 0.55 V and 0.6 V, respectively. Fig. 10 demonstrates the transient response time and the $V_{\text{out}}$ behavior when the load changes suddenly from 10 μA to 200 μA while the opposite load transition is explained in Fig. 11. It can be seen that $V_{\text{out}}$ follows $V_{\text{ref}}$ quickly with the aid of the proposed CM scheme where the higher clock frequency is employed. Table I compares this work with other state-of-the-art DLDOs.
The proposed DLDO is implemented for ultra-low-power applications. The tested chip is fabricated in 65 nm CMOS technology. The proposed CM scheme addresses the trade-off issue between fast response time and current efficiency. The test chip operates at 0.6 V with 0.55 V output voltage, and covers a load range from 10 μA to 200 μA with 99.7% current efficiency at 200 μA. The implemented chip is fully integrated with an on-chip decoupling capacitor of 100pF. The proposed DLDO is applicable to various ultra-low power applications such as biomedical systems, IoT systems, etc.

REFERENCES


### Table I. Comparison with state-of-the-art regulators

<table>
<thead>
<tr>
<th>Unit</th>
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<th>[7]</th>
<th>[8]</th>
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<td>130nm</td>
<td>40nm</td>
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<td>Minimum input voltage</td>
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<td>Nominal output voltage</td>
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<td>Maximum load current</td>
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<td>Load Regulation</td>
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<td>Current Efficiency</td>
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