# Nanyang Technological University – Economic Development Board Industrial Postgraduate Programme (NTU- EDB IPP)

**Project details**

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| NTU Faculty | Prof. Boon Chirn Chye |
| NTU Faculty's email contact | ECCBOON@NTU.EDU.SG |
| School | EEE |
| Collaborating Company | GLOBALFOUNDRIES |
| IPP Project title | 5G/6G AND BEYOND IC DESIGN |
| Description of IPP Project | To design a circuit/system to enable 5G/6G AND BEYOND IC DESIGN depending on the candidate's background and interest. The research will encompass design, simulation and measurement of circuit/system design. Candidates are encouraged to generate patents among other research output related to this work. |
| Requirements | Background in IC design. |
| Duration of the project | 4 years |
| Period of the project | 08/2022 - 07/2026 |

**Project details**

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| NTU Faculty | A/P Poenar Daniel Puiu |
| NTU Faculty's email contact | epdpuiu@ntu.edu.sg |
| School | EEE |
| Collaborating Company | GLOBALFOUNDRIES |
| IPP Project title | ESD/LU solutions for HV/RF applications in BCD/SiGe technology |
| Description of IPP Project | The main target of the project is to develop and test efficient ESD/LU device structures for High Voltage (HV) -for automotive and industrial applications- and/or for RF applications using BCD (Bipolar-CMOS-DMOS) and SiGe CMOS technologies. For this purpose the PhD candidate will become familiar with, and use GlobalFoundries's technology, namely the 40~55nm processes with 1.2V/3.3V for logic/RF and 20~120V for HV.<br><br>For this purpose, the Ph.D. student will:<br>1) Perform a thorough Literature Review to understand the existing state-of-the-art, its features and its limitations. At the same time (s)he will have to familiarize himself in depth with GobalFoundries's fabrication processes.<br><br>2) Perform calculations for the design of the desired devices, followed by Design of Experiments (DOE) and TCAD simulations & optimizations in order to find the optimal device(s) designs/structures, as well as determine their fabrication process steps and their operational characteristics. To familiarize himself/herself with such TCAD, the student can register for prof. Daniel's M.Sc. course teaching Virtual Wafer Fabrication, and of course continue to learn the softwares in GF.<br><br>3) Participate and assist in the fabrication of the designed devices.<br><br>4) After fabrication, the student will perform all the necessary tests & measurements for product characterization, followed by data analysis and - if necessary- perform a re-design.<br><br>The Ph.D. student activating in this project will have full support from the entire GF-ESD team which also has all the equipment, fabrication facilities, testing tools, etc., necessary for the work mentioned above.<br><br>GF offers a unique competitive research work environment and excellent future job & career prospects. As for any IPP based Ph.D., the candidate must be local/PR and show proof of a CGPA (based on all the grades obtained until now) of at least 4 or above. |
| Requirements | B.Sc. or M.Sc. graduate (or graduating very soon, in June 2022) |

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| Duration of the project | 4 years for PhD<br>2 years for Master by Research |
| Period of the project | 09/2022 - 12/2026 (PhD)<br>09/2022 - 12/2024 (Master by Research) |

**Project details**

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| NTU Faculty | Prof. Dong Zhao Yang |
| NTU Faculty's email contact | zy.dong@ntu.edu.sg |
| School | EEE |
| Collaborating Company | GLOBALFOUNDRIES |
| IPP Project title | Smart cost savaging with fabrication equipment monitoring and predictive maintenance using artificial intelligence technologies. |
| Description of IPP Project | This project is to develop advanced technologies for monitoring and predictive maintenance on fab equipment, specifically,<br>• Using advance ML/Data analytic to monitor the life expectancy of fab running equipment; and<br>• Achieving Smart Cost Saving: With good prediction will help to extend the maintenance cycle hence achieving cost savings. |
| Requirements | Honours degree in electrical engineering or computer science or relevant areas; capable of programming, good analytical and writing skills. |
| Duration of the project | 4 years for PhD<br>2 years for Master by Research |
| Period of the project | 08/2022 - 07/2026 (PhD)<br>08/2022 - 07/2024 (Master by Research) |

**Project details**

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| NTU Faculty | Prof. Tan Chuan Seng |
| NTU Faculty's email contact | tancs@ntu.edu.sg |
| School | EEE |
| Collaborating Company | GLOBALFOUNDRIES |
| IPP Project title | GeSn Materials and Single-Photon Avalanche Photodiode (SPAD) |
| Description of IPP Project | The end goal of this proposal is to develop a manufacturable, high sensitivity and high operation temperature germanium-based single-photon avalanche photodiode (SPAD), which is able of detecting single-photon in the short-wave infrared (SWIR is defined as 1,100~2,500 nm) region for a plethora of quantum photonic and sensing applications.<br><br>While silicon (Si) SPAD has demonstrated high performance in the spectral range below 1,000 nm, however, there are strong demands to extend the detection capability of Si SPAD detectors into the above SWIR range, which remains a challenge.<br>The proposed SPAD is based on Ge (and potentially GeSn) absorption layer and Si multiplication layer coupled with a vertical optical cavity. Thanks to the group-IV alloys, the photon absorption wavelength can be extended to the SWIR range and the absorption coefficient is increased significantly.<br><br>Furthermore, in contrast to conventional photodiodes, by coupling the Ge/GeSn SPAD with an optical cavity, SPAD with even a thin absorption layer is able to demonstrate respectable quantum efficiency, resulting in a high sensitivity and low-noise SPAD.<br><br>Based on our preliminary modeling and characterizations, we estimate that the GeSn SPAD would have high detection efficiency and its noise can be reduced significantly by novel substrate engineering method.<br><br>Low-noise SPAD allows operation at higher temperature, which is important for transferring the device from labs to practical applications. In addition, since the fabrication of the proposed SPAD is compatible with mainstream silicon CMOS technology, the cost of the device is expected to be lower than the currently used III-V material SPAD. High-performance SPAD devices in the SWIR regime are key enablers for a myriad of emerging applications include communication, quantum computing, LIDAR, fluorescence medical imaging, and others.<br><br>The success of this proposal would greatly impact social economy, healthcare, communication, autonomous system, and the related industries. |
| Requirements | Bachelor Degree in Electrical, Electronics, Materials Science, Physics or related; Strong interest in semiconductor material, processing and devices |

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| Duration of the project | 4 years |
| Period of the project | 08/2022 - 07/2026 |

**Project details**

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| NTU Faculty | Prof. Tan Eng Leong |
| NTU Faculty's email contact | eeltan@ntu.edu.sg |
| School | EEE |
| Collaborating Company | GLOBALFOUNDRIES |
| IPP Project title | Design and Analysis of Automotive Electronic Devices with 3D Integrated Circuits. |
| Description of IPP Project | With the fast-growing trends on the automotive market and technology advancement, the vehicle todays integrated with tons of electronic devices. Majority of the mechanical devices available in the vehicle are supported by electronics. Hence, the automotive electronics devices are expected to be dominated in the vehicle over the years to support fully autonomous driving, secure and high-speed communications and infotainment, and all-electric vehicles.<br><br>Since the electronics content within the vehicle is growing rapidly on the same vehicle size, the demands on higher density, higher reliability, higher bandwidths, and lower power consumption are accelerated. As such, the 3D-IC is a very promising technology where it allows the stacking of multiple chips in the vertical direction to improve the overall performance and reducing costs in a smaller footprint. Despite the advantages of 3D-IC, the challenges on 3D-IC may involve on the following's points:<br>• Complex design and test flow<br>• The trade-off of power, performance, and area (PPA) on the vertical dimension<br>• Reliability on each functional chips due to power and thermal challenges<br><br>This project will focus on research and development of the design for manufacturability' solutions to address the current challenges on 3D-IC design based on automotive aspect. |
| Requirements | Circuit design and analysis skills, EDA software |
| Duration of the project | 4 years |
| Period of the project | 08/2022 - 08/2026 |

**Project details**

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| NTU Faculty | Prof. Wang Qijie |
| NTU Faculty's email contact | qjwang@ntu.edu.sg |
| School | EEE and/or SPMS |
| Collaborating Company | GLOBALFOUNDRIES |
| IPP Project title | Miniaturized on-chip spectrometers for sensing Applications. |
| Description of IPP Project | For this project, we aim to harness randomness of disordered photonic designs in silicon or Si/Ge photonic platforms or other advanced material systems to build miniaturized photonic spectrometer with high spectral resolution and sensitivities.<br><br>You will have the opportunity to work in world-class laboratories in NTU and MNC to carry out the joint research.<br><br>You will be trained from semiconductor materials, cleanroom processing and device fabrication, electrical and optical device characterizations. Depending on your interests, you may focus on theory or experiments or both for your PhD studies with great potential to enter both industry and academia after graduation. |
| Requirements | Bachelor degree or master degree in Electrical, Electronics, Materials Science, Physics or related;<br><br>Strong interests in semiconductors, devices, photonics and systems. |
| Duration of the project | 4 years |
| Period of the project | 08/2022 - 07/2026 |

**Project details**

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| NTU Faculty | Asst. Professor Chae Sanghoon |
| NTU Faculty's email contact | sanghoon.chae@ntu.edu.sg |
| School | School of Electrical and Electronic Engineering |
| Collaborating Company | GlobalFoundries |
| IPP Project title | Low-loss LIDAR chip using 2D materials integrated photonic phased array |
| Description of IPP Project | Silicon photonics (SiPh) has made major IC breakthroughs in recent years by demonstrating a CMOS-compatible integrated photonic platform with high refractive index contrast and low cost. A scalable design for ultra-low-loss SiPh is still missing, as in most cases the optical power dissipation is due to external materials. We demonstrated that 2D materials integrated SiPh has negligible loss in a single device of the phase modulator. Our team plan to develop a new low-loss Light detection and ranging (LIDAR) chip to enable the next generation of autonomous systems. Full LIDAR chip will be consisted of optical phased arrays based on 2D materials integrated phase shift units. |
| Requirements | A Bachelor (or Master) degree in electronic engineering, materials science and engineering, who are interested in IPP in GF (as GF employees). Experience with semiconductor processing, optoelectronic and photonic devices is a plus. |
| Duration of the Project | 4 years |
| Period of the Project | 08 / 2022 – 07 / 2026 |