CE/CZ 3001 – Advanced Computer Architecture

Course Code	CE/CZ 3001
Course Title	Advanced Computer Architecture
Pre-requisites	CE/CZ 1006: Computer Organisation and Structure
No of AUs	3
Contact Hours	TEL(LAMS) 10 Lecture 26 Tutorial 10 Laboratories 5

Course Aims

This course aims to develop your understanding in the fundamental concepts and in-depth understanding of design principles of a computer system by addressing key issues in instruction set design, micro-architecture design along with the interaction of hardware components in a computer system. This course aids you to acquire necessary skills for analysing and estimating the performance of computing systems, and to design high-performance computing systems. In this course, there is a strong emphasis on the study of techniques for improving the power efficiency of single and multiple processor systems. Students will complete this course with a useful appreciation and understanding of processor design issues relating to simplicity of implementation, performance-enhancement techniques, and power-reduction methods.

Intended Learning Outcomes (ILO)

By the end of this course, you (as a student) would be able to:

1. Interpret the performance of a processor based on metrics such as execution speed and power.
2. Design processors that achieve the desired performance in a step by step manner.
3. Design and describe pipeline data-path for performance enhancement.
4. Predict the challenges of realizing different kinds of parallelism (such as instruction, data and thread level) and leverage them for performance advancement for the present, and in the future.
5. Design cache that takes into account the importance of efficient memory design and virtual memory to overcome memory wall.
6. Develop high performance programs by taking into consideration data-path, memory design and parallelism at instruction, data and thread level.

Course Content

	Topics	LAMS (Hours)	Lectures & discussion (Hours)	Tutorial (Hours)
1	**Introduction and Background:** Review of basic computer architecture, Technology trend and design goals, Performance metrics and performance enhancement techniques, Key concepts of parallel processing and pipelining, Power dissipation in processors, power metrics, and low-power design techniques.	1	4	2
2	**Instruction set architecture design:** Instruction set design: implementation and performance perspectives, relative advantages of RISC and CISC instruction sets. Relation of ISA to assembly, and to compiler, Instruction formats and addressing modes.	1.5	3	2
3	**Micro-architecture design:** Single and multi-cycle data path design. Hardwired and micro-programmed control design. Pipeline data-path.	1.5	4	1
4	**Memory Systems and I/O design:** Memory hierarchy, Cache design considerations, instruction vs. data caches, write-policy and replacement policy, analysis of cache performance, and cache design for performance enhancement, memory technologies (SRAM, DRAM, and flash memory), Virtual memory, TLB.	2	5	2
5	**Instruction-Level Parallelism:** Concept and examples of data-dependence, Challenges in ILP realization, Pipeline hazards and their solutions, Data forwarding, Register renaming, Reordering of instructions, Out-of-order execution, Branch prediction, dynamic scheduling, Limitations of scalar pipelines, VLIW and superscalar processors, Instruction, data and memory-flow challenges in superscalar and out-of-order processors.	2	5	2
6	**Data-Level Parallelism:** Introduction to vector architecture, SIMD instruction set extensions, GPU architecture.	0.5	2	1
7	**Thread-Level Parallelism:** Motivation for multicore and many-core systems, Amdahl's law under power constraint, Challenges in efficient multi-core system design, Cache coherence problem.	0.5	2	0
8	**Emerging Computing Trends:** Application specific architectures: ASIP. FPGA and ASIC. Heterogeneous multicore platform. Introduction to domain-specific computing. Comparison of performances and power consumption of general purpose processors, DSP, GPU, FPGA, and ASIC.	1	1	0
		=10	=26	=13

Assessment

a) Final Examination: 60%
b) Laboratory quizzes: 30%
c) Laboratory Assignment: 10%

CE 3002 – Sensor Control and Interfacing

Course Code	CE 3002								
Course Title	Sensor Control and Interfacing								
Pre-requisites	CE 2004: Circuits and Signal Analysis								
No of AUs	3								
Contact Hours	TEL(LAMS)	0	Lecture	26	Tutorial	13	Laboratories	5	

Course Aims

The course aims to develop in you the ability to analyse the process of sensing, control and interfacing. The signals from environment are mostly analog in nature. A proper sensing, signal conditioning and acquisition (including digitization) set up is required to prepare such signals for analysis. The acquired signals after analysis can also be used for controlling plants in a control system by measuring the error. The analysis and design of discrete control systems is an essential part of the skills of a computer engineer.

The course aims in providing strong foundation knowledge of sensors, signal conditioning, digital interfacing, sampled data system, digital control system design and system analysis for the design of signal acquisition systems and digital control systems.

Intended Learning Outcomes (ILO)

By the end of this course, you (as a student) would be able to:

1. Discuss and examine the operation of the various modules used in a signal acquisition and control system.
2. Design of signal conditioning circuits and data acquisition systems based on the signal requirements.
3. Analysing and translating the design of a personal computer based signal acquisition system in a step by step manner.
4. Review sample data systems (z-transform, closed-loop system characteristics).
5. Recognize and analyse the characteristics of discrete linear time invariant systems.
6. Analyse response for control evaluation
7. Recognize and analyse the design and implementation of discrete PID controller

Course Content

S/N	Topic	Lecture (Hours)	Tutorial (Hours)
1	**Overview of electronic instrumentation and control systems:** Transducers, Signal Conditioning, Interfacing and Control	1	-
2	**Transducers:** Passive and Active transducers, Characteristics of transducers, Resistance Temperature Detector (RTD), RTD-Wheatstone Bridge circuit, Capacitive transducers for pressure and displacement measurement, Accelerometers and their applications, Piezoelectric transducer for ultrasound medical imaging, Infrared Plethysmograph for monitoring blood volume changes and heart rate.	3	2
3	**Signal Conditioning Circuits:** Amplifier circuits: Summation amplifier, Difference amplifier, Instrumentation amplifier, Design problem. Filter circuits: Frequency response, Low-pass, High-pass, Band-pass and Band-reject Filters, Frequency Response Op-Amp specifications: Common-Mode Rejection Ratio, Slew Rate and Gain-Bandwidth Signal conditioning circuit design	6	3
4	**Digital Interfaces:** Analog-to-Digital Converter (ADC), Sampling, Aliasing, Quantization, ADC Resolution, Dynamic Range, Practical considerations, Commercial ADC – AD0820, Digital-to-Analog Converter (DAC)	4	2
5.	**Introduction to control system** Example of a digital control system, System Models, Control objective, computer control, sample data system	2	1

	The z-transform: Definition, relationship with Laplace transform Transfer function: Closed-loop systems – characteristic equation.		
6.	**Design of Digital Control** Physical realizability, Digital PI, PD, PID controller, Pole-placement design.	5	2
7.	**Linear Discrete Data System** Controllability, observability, relationship between controllability and observability, Stability: Definition, stabilizability Stability test: Routh-Hurwitz test, Jury's test Frequency-domain: Nyquist stability, Gain margin, Phase Margin	4	2
	TOTAL	=26	=13

Assessment

a) Final Examination: 60%
b) Laboratory Project: 40%

CE 3003 – Microcontroller Programming

Course Code	CE 3003							
Course Title	Microcontroller Programming							
Pre-requisites	CE/CZ 2005: Operating Systems							
No of AUs	3							
Contact Hours	Lectures/TBL	26	TEL	0	Tutorials	7	Labs	12

Course Aims

This course aims to equip you with a general understanding of microcontroller architecture and microcontroller programming methods (with and without operating systems) using ARM Cortex-M3 microcontroller as an example. You will learn about the role of microcontrollers in embedded systems and their effective utilization to meet system performance requirements.

This course is ideal if you are interested in computing hardware and its programming. The course content will focus on ARM Cortex-M3 microcontroller and Micrium OS-III real time operating system, but you will also develop an understanding of transferable knowledge to work with other microcontroller architectures and real time operating systems in the industry.

This course will help you in finding industry jobs in embedded systems and electronic product design markets. If interested in research, this course will trigger your imagination with respect to microcontroller architecture development and real-time operating system requirements.

Intended Learning Outcomes (ILO)

This course introduces microcontroller programming at an intermediate level. Upon the successful completion of this course, you shall be able to:

1. Differentiate the various versions and features of the components in ARM microcontroller architecture
2. Program microcontrollers for simple embedded system tasks with a good understanding of underlying hardware architecture and system performance requirements
3. Develop efficient embedded software based on code optimization techniques.
4. Describe and discuss Real Time Operating System (RTOS) concepts and their importance in designing real time systems.

Course Content

	Topics	Lectures/ TBL (Hours)	Tutorials (Hours)	Labs (Hours)
1	**Microcontroller Architectures** Von-Neumann vs. Harvard vs. modified Harvard architecture. RISC vs. CISC and their influence on programming and memory density. Linear vs. segmented. Memory management strategies.	2		3
2	**Cortex-M Architecture** Introduction to ARM architecture, User vs. Supervisor modes. Stack overflow and protection. ARM architecture, specifically ARMv4 to Thumb and Thumb-2. ARM Cortex-M3 address space, registers, interrupt handling, operating characteristics, operating modes, instruction set	8	2	3
3	**Compiler optimizations** Compiler optimisations for speed, memory size or balanced. Common sub-expression elimination, loop unrolling, function in-lining, code motion, dead code removal. Promotion rules. Type based alias analysis, static clustering.	2	1	
4	**Efficient Real-time 'C' Programming Techniques** Re-locatable and re-entrant software. State Machine programming, Stack pointers and frames, program-counter relative, stack relative, bit-banding, built-in function, 'orthogonal' instructions.	2	1	
5	**Linking 'C' with Assembler and Libraries** Separate compilation. External functions. ARM APCS. C99. Parameter passing. Macro assembler. Supporting legacy code. Libraries and device drivers. Pragmas and in-line code.	2		
6	**Programming Peripherals and Subsystems** Configuration of multi-function pins and 'ports'. Parallel input/output port, configuration, signal levels and drive capability. Counters, counter arrays, output compare and input capture. Pulse-width modulation. Serial interfaces for media, automotive and industrial automation. Ethernet and radio frequency links (E.g. Zigbee).	2		3
7	**Handling Multiple Tasks in Real-Time** Real-time, Polled operation vs. interrupts. Foreground vs. background. Maskable vs. non-maskable interrupts. Interrupt service routines (ISRs) and Exceptions Handlers, Nested Vectors, Tail-chaining. Multithreaded Programming, Context switching. Multi-tasking.	4	2	

8	**Real-Time Operating Systems** Task management and priority. Pre-emptive vs. Round-robin scheduling. Semaphores and mailboxes. System Tick. Kernel services and event timers. OS-based application development	4	1	3
	Check for Hours	=26	=7	12

Assessment

a) Final Written Examination: 60%
b) Laboratory Quiz: 30%
c) Team Based Learning (TBL) Activity: 10%

CE 3005 – Computer Networks

Course Code	CE 3005							
Course Title	Computer Networks							
Pre-requisites	CE/CZ 1011: Engineering Mathematics I CE/CZ 1012: Engineering Mathematics II							
No of AUs	3							
Contact Hours	Lectures	26	TEL	0	Tutorials	13	Laboratories	8

Course Aims

This course serves as a foundation for computer and communication networks. Emphasis is placed on concepts, protocols and technologies, which formulate various Local Area Networks (LANs), Wide area Networks (WANs), and their interconnections. Emphasis is also placed on the fundamentals of the Internet, and includes laboratory sessions on socket programming. Advanced materials, such as, cloud computing, will also be covered to prepare you well for your future career.

Intended Learning Outcomes (ILO)

Upon the successful completion of this course, you shall be able to:

1. Conduct network performance analysis.
2. Implement network applications via socket programming.
3. Set-up and Deploy IP networks in an organisation.

Course Content

	Topics	Lectures (Hours)	Tutorials (Hours)
1	**Computer Network Concepts** Computer Network Architecture: OSI Protocol Reference Model, TCP/IP Model; Protocols and standards at different layers; Encapsulation, fragmentation/reassembly, and multiplexing.	2	1
2	**Network Types and Performances** Types of Networks: circuit switching versus packet switching, virtual circuit switching versus datagram switching; Performance analysis of packet-switched network: M/M/1 queuing system.	2	1
3	**Data Link Layer** Concept of node-to-node communication service; Functions of Data Link Layer: flow control and error control; Performance analysis of various flow controls and ARQs; High-level Data Link Control (HDLC) protocol.	5	3
4	**Local Area Networks** LAN topologies; Medium Access Control (MAC) protocols: IEEE 802 standards; Performance analysis of LANs; Interconnecting devices: Hubs, Bridges, Switches.	5	2
5	**Network Layer** Concept of host-to-host communication service; Internet Protocol (IP): connectionless service, addressing, subnetting, subnet masks, ARP, RARP, BOOTP, NAT. Interconnecting devices: Routers; Routing protocols: RIP, OSPF, BGP.	5	3
6	**Transport Layer** Concept of process-to-process communication service and port numbers; TCP: connection-oriented service with flow-control, error-control and congestion-control; UDP: connectionless service.	4	2
7	**Application Layer** Socket: interface between process and transport layer; Socket programming with TCP and UDP; the Web and HTTP, cloud computing and data center networking.	3	1
		=26	=13

There is a total of 3 laboratory sessions, covering the above topics. There is an additional Lab session that introduces the student to Cloud computing.

Assessment (includes both continuous and summative assessment)

a) Final Examination: 60%
b) Laboratory session 1: 20%
c) Laboratory session 2: 0%
d) Laboratory session 3: 20%

CE 3006 – Digital Communications

Course Code	CE 3006							
Course Title	Digital Communications							
Pre-requisites	CE/CZ1011: Engineering Mathematics I CE 2004: Circuits and Signal Analysis							
No of AUs	3							
Contact Hours	Lectures	26	TEL	0	Tutorials	13	Lab Sessions	6

Course Aims

This course discusses on fundaments and applications of digital communication systems. The specific aims of the course are to provide you with

- the basic principles of digital communications,
- an understanding of the theoretical basis underlying the operation of common digital communication systems,
- the foundation for the study of advanced communication systems,
- various trade-offs in the design and in the resource allocation for a practical digital communication systems.

Intended Learning Outcomes (ILO)

This course introduces basics of digital communications at an undergraduate level. Upon the successful completion of this course, you shall be able to:

1. Identify different types of communication signals and their characteristics;
2. Explain different stages of baseband processing for digital signal transmission and reception;
3. Illustrate different band-pass modulation and demodulation methods for digital communication systems;
4. Recognize the importance of source coding in digital communication systems and various practical methods for source coding in practice;
5. Identify the importance of channel coding in digital communication systems and design various channel coding and decoding methods used in practice;

Course Content

	Topics	Lectures (Hours)	Tutorials (Hours)	Lab Sessions (Hours)
1	**Introduction** Basic modes of communication, Types of communication systems, Why digital communication systems, Model of a communication system, Design challenges, overview of the course.	1	0	0
2	**Signals and spectra** Classification of signals, random signals, noise in communication systems, signal transmission through linear systems.	4	3	2
3	**Baseband modulation, demodulation/detection** Formatting analogy Signals: sampling and quantization, Baseband modulation methods (PCM, DPCM, DM), SNR, Detection of binary signals in Gaussian noise, Inter-symbol interference, equalization	4	3	2
4	**Band-pass modulation, demodulation/detection** Band-pass modulation/demodulation techniques (ASK, FSK and PSK), Coherent and non-coherent detection (PSK and MPSK), Error performance for binary systems, bit versus symbol error probabilities.	5	3	2
5	**Source coding** Entropy, Source coding for digital data, Entropy (lossless) coding (Example: Huffman coding), Optimality of codes, Applications of source coding.	4	1	0
6	**Channel coding** Introduction to error control codes, Linear block codes and its properties, Generator and parity check matrices for linear block codes, error patterns and syndrome, standard array and syndrome decoding, cyclic codes, encoder design for cyclic codes, syndrome polynomial, decoders for cyclic codes, examples of channel codes.	7	3	0
7	**Challenges in communication system design** Modulation and coding trade-offs, Allocation of communication resources.	1	0	0
	Check for Hours	=26	=13	6

Assessment (includes both continuous and summative assessment)

a) Final Examination: 60%
b) Mid-term test: 20%
c) Lab Quizzes: 20%

CE 3007 Digital Signal Processing

Course Code	CE 3007							
Course Title	Digital Signal Processing							
Pre-requisites	CE 2004: Circuits and Signal Analysis							
No of AUs	3							
Contact Hours	Lectures	23	Tutorials	13	Lab	10		

Course Aims

Digital Signal Processing (DSP) has extensive applications as the building block of feature extractions for any data analytics work regarding signals. The aim of this course is to provide you with a strong understanding of digital signal processing fundamentals so that you can:

i) apply its concepts to relevant field of interest.

ii) grasp technical literature of this field,

iii) be prepared for the study of more advanced topics and applications.

Intended Learning Outcomes (ILO)

Upon completion of the course, the students should be able to:

Describe and analyse various important discrete time signals, e.g, delta, unit step, complex exponential, etc.
Discuss characteristics of discrete-time signals and systems, describe the various relationships between the input and output via convolution, frequency response, transfer function, difference equation, block realization of the system. How to generate the impulse response from a given system description.
Interpret frequency representation by Fourier Analysis and review continuous time Fourier Analysis, compute, analyse and understand the representation of signal spectra using DTFS, DTFT and DFT.
Interpret and analyse Z-Transform, its relationship to DTFT, and apply it to get transfer function and frequency response, as well as pole-zero plots, and its relationship to stability of the system.
Determine sampling rate requirements and interpret effects of aliasing.

Design Finite Impulse Response (FIR) and IIR (Infinite Impulse Response) filters and implement FIR and IIR digital filters using different structures such as direct and cascade forms in DSP processors.

Course Content

Week	Topics	Course LO	Readings/ Activities
1	**Discrete-time Signals** Introducing the important discrete time signals, interpreting angular frequency, operations on discrete time signals, characteristics of signals	1	Lectures (2Hours), Tut 1 Lab 1
2	**Discrete-time Systems** Linear time invariant systems and their properties – Convolution equation, relationships between input and output – using impulse response, difference equations, frequency domain representation, transfer function. Response of LTI systems to sinusoidal (eigen function) signals	2	Lectures (2 hours), Tut 1 Lab 2
3,4	**Frequency Analysis of Signals and Systems** Interpreting Frequency Analysis, Review of continuous time Fourier Series (CTFT), continuous time Fourier Transform (CTFT), relationship between CTFS to CTFT Introducing various CTFS/CTFT pairs, Properties of CT Fourier Transform	3	Lectures (3 hours) Tut 2A
5,6	**Discrete Time Fourier Analysis** Introducing discrete time Fourier Series (DTFS), discrete time Fourier Transform (DTFT), relationship between DTFS and DTFT. DTFT and DTFS Pairs and Properties Introducing DFT - Fourier representation of finite duration sequences – Frequency domain sampling – Properties of DFT – Circular convolution – Implementing LTI systems using DFT (zero padding and overlap-save)	4	Lectures (4 hours), Tut 2B Lab 3
6,7	**Z-Transform** What is Z-Transform – ROC and Z-Transform Pairs – Stability, Relationship of z-transform to DTFT, impulse response, and difference equations.	3	Lectures (3 hours), Tut 3
8 and 9	**Sampling and Reconstruction** Sampling - Spectrum representation - Shannon sampling theorem – Aliasing - Up-sampling and down-sampling – Introduction to audio codecs	5	Lectures (4 hours), Tut 4 (2 hours) Lab 4

10 to 12	**FIR and IIR Filter Design** Linear Phase Filter, ideal frequency selective filters, Windowing design technique for FIR Filter. IIR Filters - Butterworth filters, analog filter transformations, IIR filter design by impulse invariance, bilinear transformation – Digital signal processor implementation of these filters	6	Lectures (6 hours) , Tut 5+6(part) (3 hours) Lab 4
13	**Digital Filter Structure** Filter Structure - Direct Form I and II structures, cascade structures, parallel structures – Practical realisations using software implementation and DSP processors	6	Lectures (2 hours), Tut 6 (1 hour)
	Lecture : 26 hours, Tut : 13 hours		

Assessment (includes both continuous and summative assessment)

a) Final Examination: 55%
b) Class Quiz: 20%
c) Lab: 25%