



A Pipelined Educational Simulator

for the ARM Processor

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The screenshot displays the simulator's interface with several key components:

- Pipeline View:** A grid showing instruction progress through stages (IF, ID, EX, ME, WB) over 12 cycles. Instruction 3 shows a stall (S) in the IF stage.
- ARM Code:** A text area containing assembly instructions:


```
ADDI R1, R1, 1
ADDI R2, R2, 8
CBNZ R2, forward
ADDI R1, R2, 4
ADDI R0, R6, 2
forward SUBI R1, R2, 4
STUR R1, [R2, 20000000]
LDUR R0, [R2, 20000000]
MOV R3, #20
```
- Memory Register:** A table listing registers r0 through r15 and CPSR, all with a value of 0.
- Memory I/O:** A grid showing memory access patterns across addresses from 0x00 to 0x3e.
- Outcome:** Performance statistics including:
 - Number of cycles: 12
 - Number of RAW: 2
 - Number of Stalls: 1
 - Number of Instructions: 7
 - Number of WAR: 1
 - Number of Iterations: 0
 - Steady State CPI: 1.1428571428571428
 - Number of WAW: 0
 - Number of Control Hazards: 1
 - Number of Previous Target: 0

Introduction:

It is an educational simulator that can be an interventive tool for training and a diagnostic tool for analysis and processes. Students studying Advanced Computer Architecture can use the simulator to learn ARM architecture and explore the subject with ease.

Purpose:

To develop an educational simulator tool to display a pipelined ARM processor. It will assemble ARM instructions and display ARM pipeline and memory registers.

Problem:

There are many simulators available on the Internet related to ARM Architecture. However, some have lesser visual aids to show the pipelined cycles of the RISC architecture. Furthermore, some have limited features for learning Advanced Computer Architecture.

Solution:

To create a web application to act as an educational simulator to enable students to have fun learning Advanced Computer Architecture. The software stack used includes HTML, CSS, C#, and JavaScript.

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