NANYANG TECHNOLOGICAL UNIVERSITY SINGAPORE

School of Computer Science and Engineering
College of Engineering

Educational Simulator for analysing Pipelined RISC architecture

Project Objective

Design and Implement an Educational simulator to aid students with the understanding of computer architecture.

Simulator Features:

- Standalone Data and Control Hazards Checker
- Branch Prediction Technique
- More Data and Control Dependency Settings

Project benefits:

- Students can have more control over the Pipelined architecture Datapath through the Data and Control dependency Settings
- Standalone Data and Control Hazards provide detail on number of stall cycle needed for correct execution
- Pipelined processor Simulation provide branch prediction details

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