A 32kb 9T SRAM with PVT-Tracking Read Margin Enhancement for Ultra-low Voltage Operation

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Outline

- Introduction to ultra-low power SRAMs
- BL leakage in conventional 8T SRAMs
- Proposed 9T SRAM cell
- Proposed read margin enhancement technique
- 32Kb SRAM test chip measurement
- Conclusions
• Ultra-low power (ULP) SRAMs are indispensable for many ULP SoCs with budget energy
• Energy efficiency is a key figure of merit
• Ultra-low voltage operation is required, but challenging

*N. Verma, TVLSI, 2010*
Introduction

- At ULV, 6T SRAM fails to operate due to degraded margins.
- Decoupled SRAM cells (7T, 8T, 9T, etc.) have been proposed for improved stability.
- Single ended 8T SRAM cell is the most popular.
- In 8T SRAM, data-dependent leakage limits the sensing margin.
BL Leakage Issue in 8T SRAM

- Pull-down BL leakage limits RBL sensing margin
- Worst case for reading ‘0’ occurs at minimum BL leakage
- Worst case for reading ‘1’ occurs at maximum BL leakage

Condition for positive sensing margin

\[ I_{\text{cell}_0} + I_{\text{leak}_\text{min}} > I_{\text{cell}_1} + I_{\text{leak}_\text{max}} \]
BL Leakage Issue in 8T SRAM

- At nominal VDD, $I_{on}$ is much larger than $I_{off}$
- At ULV (VDD ≤ $V_{th}$), $I_{off}$ becomes comparable to $I_{on}$, thus BL sensing is susceptible to error
- For example, at 0.25 V, $I_{on} \approx I_{off}$ at 256 cells per BL in the worst case condition
BL Leakage Issue in 8T SRAM

- At 0.40 V, 8T SRAM with 256 cells per BL has reasonable sensing margin
- A 0.25 V, sensing margin is negative in the worst case scenario
Proposed 9T SRAM cell

- Decoupled SRAM cell and 3T read port
- The read/write operation is similar to normal 8T SRAM
- Equalized leakage current through the 3T read port
- Either $N_1-N_2$ or $N_1-N_3$ will leak from RBL to ground depending on the cell data
- **BL leakage current is independent of cell data**

![New read port for Equalized bitline leakage](image-url)
Proposed 9T SRAM: Sensing Margin

- Reading ‘1’: \( I_{BL-0} = I_{\text{cell}_1} + I_{\text{leak}} \)
- Reading ‘0’: \( I_{BL-1} = 0 + I_{\text{leak}} \) → Sensing Margin = \( I_{\text{cell}} \)

Theoretically, the proposed 9T cell provides positive margin regardless of the operating voltage.
Proposed 9T SRAM cell: $\frac{I_{\text{read}_1}}{I_{\text{read}_0}}$

- In 8T SRAM cell, $\frac{I_{\text{read}_1}}{I_{\text{read}_0}}$ diminishes to 1 at 0.28 V
- However, the proposed SRAM cell provides $\frac{I_{\text{read}_1}}{I_{\text{read}_0}} > 1$ even at 0.2 V
Proposed Boosted BL Scheme

- **Pull-up** $I_{\text{BOOST}}$ holds BLs. Final levels of $BL_1$ and $BL_0$ depend on the respective pull down current.
- Sensing margin can be optimized by tuning $I_{\text{BOOST}}$.
- Sensing window is extended for ULV operations.

![Diagram of proposed boosted BL scheme]

Conventional

Proposed

$RBL_i = \bar{V}_{\text{DD}}$

$Q_{6T}$

$Q_{6T}$

$RWL_0 = \text{VDD}$

$RWL_{255} = \text{GND}$

$V_{\text{bias}}$

$I_{\text{BOOST}}$

$P_1$

$P_2$

$V_{\text{DD}}$

$\text{ReadEn}$

$\text{PreCharge}$

$\text{WL}$

$\text{BL1/BL0}$

$Sensing\ \text{window}$

$\text{Read}$

$\text{ReadEn}$

$\text{PreCharge}$

$\text{WL}$

$\text{BL1/BL0}$

$Sensing\ \text{window}$
Optimal Bias Voltage Generator

- Two dummy columns are used to generate maximum and minimum allowable biasing voltages.
- These two voltages are averaged before applying to the main array.
RBL Boosting : Simulation Results

- The proposed SRAM cell provides static BL levels and offers a longer sensing window.
- The proposed bias voltage generator tracks PVT variations and maximizes the sensing margin.
Test Chip Architecture

- 32Kb 8T SRAM array with 256 rows and 128 columns.
- 128 columns are organized with 8 IOs and each IO has 16 columns.
- Inverter-based sense amplifier is used for simplicity with the aid of the proposed scheme.
Test Chip Measurement Results

- Read access time of 2.5 $\mu$s is achieved at 0.2 V
- $E_{\text{min}}$ of 1 pJ/access is achieved at 0.4 V
Measurement results (‘cont)

- $V_{DD_{min}}$ of the proposed SRAM is lower than that of the conventional 8T across the temperature range.
- Leakage current becomes dominant below 0.4 V
### Die Photo and Summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>65 nm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell size</td>
<td>0.52×3 µm²</td>
</tr>
<tr>
<td>Capacity</td>
<td>256×128 Kb</td>
</tr>
<tr>
<td>VDD</td>
<td>0.18 ~ 1.2V V</td>
</tr>
<tr>
<td>Access time</td>
<td>4.1 µs at 0.18 V</td>
</tr>
<tr>
<td>$E_{\text{min}}$</td>
<td>0.92 pJ @ 0.4 V</td>
</tr>
<tr>
<td>Power</td>
<td>2.6 µW @ 0.4V</td>
</tr>
<tr>
<td>Leakage power</td>
<td>1.2 µW @ 0.4V</td>
</tr>
</tbody>
</table>

The image shows a 256×128 SRAM array with decoder & driver, control & boost bias generator, and read/write & bitline boosting circuits.
Conclusions

• Ultra-low power SRAMs require robust and reliable ultra-low voltage (ULV) operations

• Data-dependent BL leakage limits BL sensing margin at ULV operation

• An energy efficient ULV SRAM is implemented by utilizing:
  – 9T SRAM cell for equalizing BL leakage
  – Bitline boosting current for improving sensing margin and sensing window