An Area- and Power-Efficient FIFO with Error-Reduced Data Compression for Image/Video Processing

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Introduction

✓ Many image/video processing algorithms require digital filtering like image enhancement, image restoration, image compression, image segmentation, and video coding in both spatial and frequency domains.
✓ Regarding the hardware implementation of image/video signal processing algorithms, many filtering operations require storing part of input image or part of previous stage results temporarily. However, it has not been comprehensively investigated to reduce the size of the temporary pixel buffers (i.e., FIFO).
✓ The size of the FIFO significantly affects the total area and power of a design. It has been reported that memory consume around 50~80% of the power consumption in many SOC (System On Chip).
✓ Two figure-of-merits (FOM) employed to measure the distortion are:
  \[ \text{MSE} = \frac{1}{n} \sum_{i=1}^{n} (I_i - Q_i)^2 \]
  \[ \text{PSNR} = 10 \log_{10} \left( \frac{\text{max}(I)}{\text{MSE}} \right) \]

Results

✓ To verify the proposed technique, we have applied the proposed FERDC technique to the FIFOs exploited in the column filtering of the 2D wavelet transform.
✓ Utilized filters:
  - 1D Cohen-Daubechies-Feauveau (CDF) 9/7 biorthogonal filters
  - Wavelet Daubechies D4 filters (db4)
✓ Ideal Case:
  - BL= 10 bits, BH= 9 bits
  - MSE<0.08, PSNR> 58 dB

Methods

✓ It employs a concept of pixel prediction where every pixel can be predicted utilizing adjacent pixels.

The Proposed FIFO Architecture

✓ In encoding part:
  - Differential Predictor: it is to remove horizontal correlations between consecutive inputs.
  - Update Error: Before sending \( y_i \) to quantizer, the energy-compacted difference is updated by the quantization error of previous difference \( (E_{i-1}) \) to prevent the quantization errors from being accumulated at the output, \( x_{1q} \).
  - Quantizer: the difference values can be quantized to b-bit integer values to reduce the data width.

✓ In decoding part:
  - Inverse Quantizer (I.Q.): it is to retrieve the data from the corresponding b-bit integer values read from FIFO.
  - Inverse Differential Predictor: The inverse differential predictor generates the output \( (x_{1q}) \) using the retrieved values.

✓ This proposed architecture reduces the FIFO width from B bits to b bits.

Summary

✓ A new FIFO architecture leading to dynamic and leakage power reduction significantly.

- MSE: 9.29 (3-bit Compression), 16.28(4-bit Compression)
- PSNR: 42.30dB (3-bit Compression), 39.52dB(4-bit Compression)
- FIFO size reduction: 30% to 44.44%
- Dynamic power reduction: 31.6% to 60.34%
- Leakage power reduction: 33% to 44.44%

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