An Improved Read/Write Scheme for Anchorless NEMS-CMOS Non-volatile Memory

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• Introduction
• Proposed NEMS-based Anchorless Memory
• Proposed Read/Write Control Scheme
• Proposed Two-level Gate Pulse
• Performance evaluation
• Conclusion
• Memory devices for harsh operating environment are highly demanded
• Market Available flash memory exhibits poor retention at high temperature( > 200°C)
Anchorless NEMS Memory Device

- Anchorless structure for device scalability
- Proposed device has three terminals (D: Drain, S: Source, G: Gate) and a shuttle
- The shuttle can be actuated between G and D-S terminals
Anchorless NEMS Memory Device

- Actuation is performed by utilizing the electrostatic force between the terminals and the shuttle.
- Data retention is realized by Van der Waals force.
- Data read-out is carried out by sensing the current between the D and S terminals.
Data Retention Principle

- Magnitude (Adhesion energy $\Gamma$) of the adhesive (Van Der Waals) force:

$$\Gamma = \frac{A_{metal}}{12 \cdot \pi \cdot D_{rms}^2}$$

- $A_{metal}$ - Hamaker constant of the metal; $D_{rms}$ – surface roughness

- $F_{ad}$ increases with temperature thus data retention gets better at higher temperature
Shuttle Actuation Principle

- New data is written by actuating the shuttle between the D-S and the G terminals.
- The required voltage to break the adhesive force is:

\[ V_p = 4d_{gap} \cdot \sqrt{\frac{\Gamma \cdot \alpha}{d_{vdw} \cdot \varepsilon_0}} \]

- \( d_{gap} \) – vacuum actuation gap; \( \alpha \) – real/apparent contact area; \( d_{vdw} \) – Van der Waals distance.
- The stored data will be flipped (i.e. \( 1 \rightarrow 0 \) and \( 0 \rightarrow 1 \)) as long as \( V_{D/S-G} > V \), regardless of the original value.
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Proposed array organization

- Array structure has:
  - 1NEMS-2T memory cell
  - One WL per row, two BLs per column similar to SRAM
  - Each column has one Gate signal for writing “0” and “1”
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• BLs are pulled to $V_{DD}$ by the PMOS (P1) switches.
• If the shuttle is at D/S (i.e. Data “1”) BLB is charged up.
**Proposed Write Operation**

- Write “1” or “0” can be done by flipping the stored data.
- If old data is different from the new data, Gate signal is triggered to flip the value.
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Proposed Two-level Gate Pulse

- Due to process variation some shuttle have shorter flight time
- Shuttle bounces if the gate pulse is longer than required
Proposed Two-level Gate Pulse

- Two-level Gate signal eliminates shuttle oscillation
- Write delay improves with the proposed scheme
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Performance Evaluation

- Delay and Power increases with temperature
- Delay can be reduced by increasing the duration of second pulse in Two-level Gate pulse
• Write delay decreases with increase in gate voltage due to increased attractive force
• As gate pulse stays longer, the delay gets reduced
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Conclusion

• A memory array implementation is proposed for the novel Anchorless-NEMS

• We propose improved read/write scheme:
  – 1 NEMS – 2 T bit cell
  – Two-level Gate signal to eliminate shuttle oscillation and to improve write delay
  – Variation tolerance is addressed