A 5.61 pJ, 16 kb 9T SRAM with Single-ended Equalized Bitlines and Fast Local Write-back for Cell Stability Improvement

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Contents

• Challenges in Ultra-low Voltage SRAMs
• Proposed 9T SRAM Cell and Bitline
• Proposed Bitline Equalization Technique
• Proposed Fast Local Write-back Scheme
• 9T SRAM Test Chip Measurement
• Conclusions
Ultra-low Power Systems

Wireless Sensors

Mobile Phones

Biomedical Devices

RF ID Tags
Challenges of Ultra-low Voltage SRAM Design

- Small Static-Noise-Margin (SNM)
- Poor write margin
- Reduced bitline sensing margin

Mainly due to small $I_{on}$-to-$I_{off}$ ratio and large current variation in subthreshold
Previous Ultra-low Voltage SRAM Design Techniques

- **SRAM Cell Stability Improvement**
  - Cross point write structure with data aware WWL [1]
  - Read buffer for read stability enhancement [1]

- **Bitline Sensing Improvement**
  - Digitized replica bitline delay [2]
  - Decoupled differential sensing [3]

- **Write-ability Enhancement**
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Decoupled 9T SRAM Bitcell

- **Read ‘1’**: a pull-up path via M9 slows down the RBL discharging
- **Stand-by**: RVDD and /SEL held to VDD to minimize leakage
- **Higher V_{th}** PMOS: better write margin

**Table:**

<table>
<thead>
<tr>
<th></th>
<th>Selected Col.</th>
<th>Unselected Col.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Read</strong></td>
<td>RWL=RVDD=VDD, WWL=/SEL=GND</td>
<td>RWL=RVDD=VDD, WWL=GND, /SEL=VDD</td>
</tr>
<tr>
<td><strong>Write</strong></td>
<td>RWL=RVDD=VDD, WWL=/SEL=VDD</td>
<td>RWL=RVDD=VDD*, WWL=VDD, /SEL=GND*</td>
</tr>
<tr>
<td><strong>Stand-by</strong></td>
<td>RWL=WWL=GND, RVDD=/SEL=VDD</td>
<td></td>
</tr>
</tbody>
</table>

*Note: Localized ‘write-back’ operation is conducted in unselected columns during write operation.*
Leakage Current in 9T SRAM Bitcell

VDD = 0.2 V, Temp. = 80°C

- Proposed leakage comparable to minimum leakage in single-\(V_{th}\) 8T bitcell
- 35% improvement in proposed stand-by leakage compared to average leakage of 8T
Hierarchical Bitline Structure

- Hierarchical bitlines to reduce delay and power
  - 64 cells/BL for area overhead consideration
- Delay improved by 37.5%
- Delay variance improved by 64.7%
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**Read Bitline Sensing Issue**

Conventional 8T SRAM in 65nm CMOS, 256 cells/BL, Temp. = 80°C

- **Reduced** $I_{\text{on}}$-to-$I_{\text{off}}$ ratio at lower supply voltage
  - Faster bitline discharging by leakage current
  - Sensing failure due to data-dependent bitline leakage
Previous Bitline Equalization

For successful sensing:
\[ I_{cell} + I_{leak_{\text{min}}} > I_{leak_{\text{max}}} \]

For successful sensing:
\[ I_{cell} + I_{leak} > I_{leak} (\text{Always true}) \]

- Constant bitline leakage* always has positive sensing margin
- Not applicable to decoupled SRAMs

* A. Alvandpour et al., *ESSCIRC*, 2003
Proposed Bitline Equalization

- Read ‘0’ -
- Read ‘1’ -

- Equalized bitline leakage in single-ended RBL

- The path of data independent bitline leakage
  - Always one on NMOS and one off NMOS
Improved Read Bitline Sensing

- **Conventional 8T**

  - Sensing margin:
    \[ I_{\text{cell}} + I_{\text{leak\_min}} - I_{\text{leak\_max}} < I_{\text{cell}} \]

- **Proposed 9T**

  - Sensing margin:
    \[ I_{\text{cell0}} + I_{\text{cell1}} \text{ (enhanced)} \]

  - Enhanced Bitline Sensing Margin

- **SRAM**
  - Conventional 8T SRAM
  - Proposed 9T SRAM
**RBL Swing and Timing Window**

VDD = 0.25V, 256 cells/RBL, TT, Temp.= 80°C,

- Improved RBL swing and timing window due to equalized bitline leakage
  - Faster discharging speed of read ‘0’ with $I_{\text{leak}} + I_{\text{read0}}$
  - Slower discharging speed of read ‘1’ with $I_{\text{leak}} - I_{\text{read1}}$
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Stability Issue of Half-selected Cells

- Write wordline (WWL) is shared by cells in a row
- Write could be enabled for half-selected cells
- Data flipping could occur in half-selected cells
Previous Solution for Half-selected Cells

- Write back scheme to eliminate half-select issue
  - Read data from unselected columns and then write back
  - Additional time for reading data in write operation is needed

*Y. Morita et al., VLSI Symposium, 2007*
Proposed Fast Local Write-back Scheme

- Four sets of local bitlines linked to global bitlines
  - Inserted read generating fast read data in local RBLi
  - Writing local RBLi data back into local WBLi/WBLBi
Proposed Fast Local Write-back Scheme

- Local read bitlines make additional read delay small enough
- Write-back speed is similar to read speed by global bitlines
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### 16kb SRAM Array

- **Capacity:** 16kb SRAM Array (256 rows x 64 columns)
- **IOs:** 4 IOs
- **Mux:** 16-to-1 Mux.
- **Write-back Delay Control**

#### SRAM Architecture

- **Row Decoder & WL Drivers**
- **Write-back Delay Control**
- **Col. Decoder & Write Drivers**

#### Control Logic

- **Read-out Circuit**

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- **16kb SRAM in 65nm CMOS technology**
- **Measurement results based on max. frequency**
- **All testing conducted at 27°C**
- Minimum operating voltage of 0.24V, at 27°C
- Read access time of 4.88 µs at VDD = 0.24V
Active Power and Leakage Measurement

- Two different slopes of write/read power
- Leakage decreases from 54 µA at 1.2V to 2.1 µA at 0.24V
• Minimum average power: 1.08 µW at 160 KHz, 0.24V
• Minimum energy point: 5.61 pJ at 600 KHz, 0.3V
Test Chip Micrograph and Summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>65nm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip Size</td>
<td>282 x 329 µm²</td>
</tr>
<tr>
<td>Cell Size</td>
<td>2.44 x 0.72 µm²</td>
</tr>
<tr>
<td>(logic design rule)</td>
<td></td>
</tr>
<tr>
<td>VDD min.</td>
<td>0.24V @ 256 rows</td>
</tr>
<tr>
<td>Read Access Time</td>
<td>4.88 µs @ 0.24V</td>
</tr>
<tr>
<td>Leakage Current</td>
<td>2.1 µA @ 0.24V</td>
</tr>
<tr>
<td>Power</td>
<td>1.08 µW @ 0.24V</td>
</tr>
<tr>
<td>Min. Energy</td>
<td>5.61 pJ @ 0.30V</td>
</tr>
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Conclusions

• Ultra-low voltage SRAMs play a key role in many ultra-low power applications.
• We propose ultra-low voltage SRAM techniques:
  – 9T Novel SRAM cell with equalized RBL leakage for improving RBL sensing
  – Hierarchical bitline optimization for reducing performance variation
  – Local fast write-back scheme to eliminate half-selected cells without performance degradation
• 9T SRAM test chips showed 5.61pJ at 0.3V.