A 5.61 pJ, 16 kb 9T SRAM with Single-ended Equalized Bitlines and Fast Local Write-back for Cell Stability Improvement

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Abstract—A 5.61 pJ, 16 kb 9T SRAM is implemented in 65nm CMOS technology. A single-ended equalized bitline scheme is proposed to improve both read bitline voltage swing and sensing timing window. A fast local write-back allows the half-select-free write operation without performance degradation. The test chip shows a minimum operating voltage of 0.24V and a minimum energy of 5.61pJ at 0.3V.

I. INTRODUCTION

Robust SRAMs with a wide operating supply voltage range are critical in many ultra-dynamic voltage scaling (UDVS) applications such as processors, implantable biomedical devices, wireless sensor nodes, and portable electronics. The primary goal of UDVS is to provide high performance during normal operation modes while significantly reducing power and energy consumption during ultra-low voltage operation modes [1], [2]. Conventional 6T SRAMs fail to deliver reliable UDVS operation due to the deteriorated Static Noise Margin (SNM), poor write margin, and reduced bitline sensing margin. In UDVS systems, decoupled SRAM cells with a dedicated read port have been employed to eliminate disturbing current from bitlines into data storage nodes and consequently to improve SNM at a cost of additional devices [3-7]. Poor write margin issues have been addressed by design techniques such as boosted wordline voltage and collapsed cell supply. Write-back schemes have been utilized in many low-voltage SRAMs for improving the stability of half-selected cells by using an additional clock cycle. The degradation in bitline sensing margin demands various read-assist circuit techniques like bitline leakage manipulation (reduction, compensation, and equalization) [5-7], a virtual-ground replica scheme [3], sense amplifier redundancy [5], etc. Although various ultra-low voltage SRAMs have been successfully demonstrated through the improved cell stability of the decoupled SRAM cells, the smaller read bitline sensing margin and the stability of half-selected cells are still remained as significant challenges to the reliable ultra-low voltage operation.

In this paper, we demonstrate a 0.3 V, 5.61 pJ, 16 kb SRAM with enhanced bitline sensing margin and improved cell stability. Circuit techniques such as a novel 9T SRAM cell, a single-ended equalized bitline scheme, and a fast local write-back scheme are proposed.

II. PROPOSED 9T SRAM: CELL AND BITLINE STRUCTURE

The proposed 9T SRAM cell is illustrated in Fig. 1. It has a dedicated read port consisting of 3 NMOS transistors (M7, M8, and M9). Compared to the conventional decoupled 8T SRAM cell, M9 is added for equalizing the read bitline leakage in unselected rows and providing a pull-up current path in a selected row to improve SNM at a cost of additional devices [3-7]. Poor write margin issues have been addressed by design techniques such as boosted wordline voltage and collapsed cell supply. Write-back schemes have been utilized in many low-voltage SRAMs for improving the stability of half-selected cells by using an additional clock cycle. The degradation in bitline sensing margin demands various read-assist circuit techniques like bitline leakage manipulation (reduction, compensation, and equalization) [5-7], a virtual-ground replica scheme [3], sense amplifier redundancy [5], etc. Although various ultra-low voltage SRAMs have been successfully demonstrated through the improved cell stability of the decoupled SRAM cells, the smaller read bitline sensing margin and the stability of half-selected cells are still remained as significant challenges to the reliable ultra-low voltage operation.

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![Figure 1. Proposed 9T SRAM cell and control.](image-url)
local bitline in consideration of the area overhead (Fig. 3). The chosen hierarchical bitline structure improves the read delay and delay variation by 37.5% and 64.7% respectively.

**III. SINGLE-ENDED EQUALIZED BITLINES**

Bitline leakage is a primary concern in reliable bitline sensing since it becomes significant compared to the SRAM cell read current, particularly at ultra-low supply voltages. This limits the number of cells in a bitline small. An equalization scheme for differential bitlines was proposed to enhance the bitline sensing ability without changing the number of cells per bitline [7]. However, the previous equalization scheme used a 6T SRAM cell and is not applicable to single-ended bitlines. Fig. 3 compares the principle of the proposed single-ended equalized bitlines with the conventional 8T SRAM bitlines. In the conventional 8T SRAM, the amount of the bitline leakage is determined by the data pattern stored in a column. When reading data ‘0’, the RBL discharging speed is determined by the summation of the pull-down read current and the constant bitline leakage. Similarly, when reading data ‘1’, the summation of the pull-up current through M8 and M9 (Fig. 1) and the constant bitline leakage controls the discharging speed. Consequently, the proposed single-ended equalized bitline provides better sensing margin in terms of voltage swing and sensing timing window (Fig. 4 (right)), which further lowers the minimum operating voltage.

**IV. FAST LOCAL WRITE-BACK FOR STABILITY IMPROVEMENT**

Figure 3. Principle of the equalized bitline.

Figure 4. Single-ended equalized read bitline for improved sensing margin.
Decoupled SRAM cells improve cell stability significantly in read operation [3-7]. Thus, the worst case cell stability occurs in the half-selected cells during write operation. The half-selected cells have the same SNM as that of the 6T SRAM cell. Pulsed wordline improves the dynamic cell stability by reducing the time period of cell node disturbance by the pre-charged write bitlines [8]. However, the pulsed wordline cannot remove the half-selection issue completely and accurate pulse width control for the reliable write operation and the minimal disturbance is remained as a challenging task. Write-back schemes can eliminate the half-selection problem by firstly reading data from unselected columns and writing the read data into write bitlines (WBLi) of the unselected columns. After the inserted read operation, a delayed write wordline (WWL) is enabled for writing target data and read data into the enabled cells. Due to the fast read operation through the local read bitlines, the additional delay for the inserted read operation is small enough to make the write-back speed similar to the read speed through the global bitlines. Consequently, the proposed fast local write-back eliminates the half-selection problem without significant performance degradation. Fig. 6 illustrates a read/write timing diagram including the proposed write-back operation.

V. MEASUREMENT RESULTS

A 16 kb SRAM with the proposed techniques was fabricated in a 65 nm CMOS technology. The 16 kb array is configured with 256 rows and 64 columns. Each column is divided into four sub-blocks for realizing the hierarchical bitline structure and the fast local write-back operation. Fig. 7 summarizes the measured read access time over different supply voltage levels. The read access time is 4.88 µs at the minimum operating supply voltage of 0.24 V. Increasing supply voltage from the minimum operating voltage reduces the read access time exponentially while the supply voltage is in the super-threshold region. When the supply voltage is in the sub-threshold region, the reduction in the read access time from the raised supply level is slowed down. Fig. 8 is a sample screenshot of the SRAM read operation. The test chip is fully functional down to 0.24V. Fig. 9 shows the measurement results of the read/write power, the leakage power, the average power, and the energy consumption from the test chip. The average write power is larger than the average read power by ~25% (Fig. 9(a)). This is primarily due to the inserted read operation required by the proposed fast local write-back operation. Note that the read/write power plots show two different slopes because the maximum operating frequency degrades exponentially at a lower supply.
the high write-back speed comparable to the normal read write-back operation through the local read bitlines facilitates proposed a fast local write-back scheme to implement half-the bitline voltage swing and sensing timing window. We also the amount of read bitline leakage. Consequently, it enhances always provides positive bitline sensing margin regardless of eliminates the data dependency of the read bitline leakage and The proposed single-ended bitline equalization scheme sensing margin and removing half-selected cells is presented. given in Fig. 10.

Figure 9. SRAM measurement results: (a) read/write power, (b) leakage current, (c) average power (50% read and 50% write), and (d) energy consumption.

A 9T SRAM with circuit techniques for improving bitline voltage region. The leakage current changes from 54 μA to 2.1 μA by lowering the supply voltage from 1.2 V down to 0.24 V (Fig. 9(b)). The average power of the test chip is 1.08uW with the maximum operating frequency at 0.24V (Fig. 9(c)). The minimum energy of 5.61 pJ was achieved at 0.3 V (Fig. 9(d)). The summary of the SRAM test chip is given in Fig. 10.

VI. CONCLUSION
A 9T SRAM with circuit techniques for improving bitline sensing margin and removing half-selected cells is presented. The proposed single-ended bitline equalization scheme eliminates the data dependency of the read bitline leakage and always provides positive bitline sensing margin regardless of the amount of read bitline leakage. Consequently, it enhances the bitline voltage swing and sensing timing window. We also proposed a fast local write-back scheme to implement half-select-free write operation. The inserted read operation and the write-back operation through the local read bitlines facilitates the high write-back speed comparable to the normal read speed. A test chip was fabricated in a 65nm CMOS technology. The hardware implementation demonstrates a minimum operating voltage of 0.24 V and a minimum energy of 5.61 pJ at 0.3 V. The proposed circuit techniques can be employed in SRAMs for UDVS systems where ultra-low voltage operation is strongly demanded.

REFERENCES