A 76% Efficiency Boost Converter with 220mV Self-Startup and 2nW Quiescent Power for High Resistance Thermo-Electric Energy Harvesting

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Presentation Outline

- Background
- Review of Startup Circuits
- Proposed Energy Harvesting Architecture
  - Proposed Power-on-Reset (PoR) Based Starter
  - PoR Characteristics and Operation
  - PoR Analyses and Design
- Measurement Results
- Conclusion
Example of a micro-scale Body Area Sensor Network (BASN)

Battery-operated circuits – cumbersome for portable network of devices

**Solution:** battery-less energy harvested systems

*http://pulse.embs.org/january-2014/forecast-2014/*
Thermal Harvesters

- Thermal energy ubiquitously available
- Suited for body-wearable applications
- Thermo-electric generators for energy harvesting
- Voltage and power from body heat suitable for µW

Model of Energy Harvesting System

- TEG from body heat produces low voltage (10-300 mV)
- Battery-less systems require Starter to “cold-start”
- Starter must use available ambient energy to kick-start
Conventional Battery-less Starters

- **Phase 1: Inductor Charged**

- **Phase 2: Discharged to COUT**

- **Design challenges:**
  - Vth of M1: difficult to turn M1 on at sub-threshold voltages
  - Fully electrical startup with minimum off-chip components
  - To generate reliable clock signals at low voltages
Review of Starters

(1) 35mV Startup (JSSC ‘09)
(2) 50mV Startup (SOVC ‘12)
(3) 40mV Startup (JSSC ‘12)

<table>
<thead>
<tr>
<th></th>
<th>(1) 35mV Startup (JSSC ‘09)</th>
<th>(2) 50mV Startup (SOVC ‘12)</th>
<th>(3) 40mV Startup (JSSC ‘12)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leakage Losses</td>
<td>MEMS switch</td>
<td>Native nMOS</td>
<td>Native nMOS</td>
</tr>
<tr>
<td>Off-chip Inductors (&gt;1)</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Start up from high ESR</td>
<td>Limited</td>
<td>Limited</td>
<td>Limited</td>
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</tbody>
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B3L-B: A 76% Efficiency Boost Converter with 220mV Self-Start-up and 2nW Quiescent Power for High Resistance Thermo-Electric Energy Harvesting
Proposed Harvesting Architecture

System Architecture

- Starter, Control Unit, Boost Converter Core
- Starter: PoR and CP; Control Unit: PGU and DS
- Charge-Pump (CP) mode: CPOUT powers PGU (VOUT<400mV)
- VOUT mode: VOUT powers PGU (VOUT>400mV)
System Operation Modes

- **Active Blocks in CP mode**
  - CP mode: M2 clocked by PGU, powered by CPOUT
  - VOUT mode: M2 clocked by PGU, powered by VOUT
  - **400mV** is kept as a safe limit for successful operation of PGU by VOUT in VOUT mode
Proposed Starter

- Starter comprises of PoR, CP, and Switch M1
- Feedback between PoR, M1 and ESR generates pulses
- CP uses PoR pulses to raise CPOUT, which powers PGU during startup
- After startup, Starter is automatically disabled
Proposed Power-on-Reset (PoR)

- Proposed PoR utilizes high $E_{SR}$ of TEG to generate pulses
- No additional clock generator is required
- PoR automatically disables itself and Starter
Operation of Proposed PoR

Phase 1: CLK1 = ‘High’
- VD<VST (INV1)
- CLK1= HIGH=VIN
- M1 is turned ‘weakly’ on

Phase 2: CLK1 = ‘Low’
- VD>VST (INV1)
- I2<I1; VIN1>VIN2
- CLK1= LOW=‘0’
- M1 is turned off
PoR Simulation

Process corner affects pulse generation in PoR

Proposed PoR is more reliable at SF corner

‘Slow’ N1 & N4 help the pulses to continue for a longer period. Similar applies for ‘Fast’ pMOS, P1

Required number of pulses in PoR for reliable startup worsens for fast nMOS corners
Leakage of Proposed Startup

- Leakage current through M1 @ VTEG=220mV is constant
- Raising VTEG decreases the leakage through M1, as near and above sub-threshold, turning on or off of M1 stronger
- The minimized leakage through M1 reduces quiescent current through Starter, and increases system efficiency
Starter Design Parameters

**CPOUT = 4.VIN - 4T \cdot \frac{T}{C}**

- **Time period** \(T = \frac{1}{f}\)
- **Start-time of pulses** \(x\)
- **Pulse length** \(y\)
- **Number of pulses** \(n\)

**Parametric Variations**

<table>
<thead>
<tr>
<th>(r)</th>
<th>VIN</th>
<th>(W/L) of (N1)</th>
<th>PoR Cap.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Increases</td>
<td>Increases</td>
<td>Increases</td>
<td>Not Affected</td>
</tr>
</tbody>
</table>

- **W/L of N1** is decided to make VST (INV1) lower than VIN/2
- **For 3-stage CP**, minimum VIN for CPOUT of 400mV is between 150-170mV considering losses
- **Minimum number of pulses** (n) is selected based on the minimum required by CP to reach 400mV
Charge-Pump Design

Charge-Pump (CP)

- CP is a 3-staged Dickson’s Charge Pump
- CPOUT rises with PoR pulses and is discharged with PoR reset
- Since PoR is essential for CP to hold state, mode transfer from CP mode to VOUT mode is necessary in steady-state
Key Circuit Blocks (PGU)

- Ring Oscillator, Frequency Divider and a Buffer form PGU
- Ring Oscillator core is a stacked-inverter-based one
- PGU powered by CPOUT (CP mode) or VOUT (VOUT mode)
- The PGU is intended to generate high duty-cycle clock
Detector is triggered at 400 mV
- Trigger is where off and on-currents equate
- Beyond \( V_{\text{trigger}} \), \( V_x \) follows \( V_{\text{OUT}} \).
Test Chip Implementation

- Chip fabricated in 65nm CMOS
- Chip area = 430 × 340µm²
- Two off-chip components: inductor and capacitor

Chip Micrograph
Measurement Results

MPG-D751 V-I Characteristics

- ΔT = 30K
- ΔT = 20K
- ΔT = 10K
- ΔT = 5K

Output Voltage (V) vs. Output Current (mA)

Startup Transient Waveforms

- Startup time: 10.5ms
- PoR/CLK1: 220mV
- VTEG: 220mV
- VOUT: Steady-state 1.3V
- CLK1 reset:
- Self-generated Pulse-train

- Minimum startup voltage from TEG is 220mV
- Startup voltage at ESR of 70Ω is 170mV
Measurement Results

Startup voltage Variation with $E_{SR}$

- Minimum startup VTEG = 170 mV at $E_{SR} = 70\,\Omega$
- Maximum ESR for startup = 450 $\Omega$
- Peak efficiency of 76% at VTEG = 180 mV
- QP stands for quiescent power in Starter

Efficiency and QP with VTEG

- Peak Efficiency = 75.9 %
## Comparison

<table>
<thead>
<tr>
<th></th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>QP (%)</strong></td>
<td>--</td>
<td>--</td>
<td>3.97</td>
<td>--</td>
<td>0.4 (4nW)</td>
</tr>
<tr>
<td><strong>Min. VIN (mV)</strong></td>
<td>--</td>
<td>--</td>
<td>30</td>
<td>--</td>
<td>85</td>
</tr>
<tr>
<td><strong>Start-up volt. (mV)</strong></td>
<td>40</td>
<td>330</td>
<td>50</td>
<td>380</td>
<td>220 (170)</td>
</tr>
<tr>
<td><strong>Peak Eff. (%)</strong></td>
<td>61</td>
<td>80</td>
<td>73</td>
<td>81</td>
<td>76</td>
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<tr>
<td><strong>Process (nm)</strong></td>
<td>130</td>
<td>--</td>
<td>65</td>
<td>130</td>
<td>65</td>
</tr>
<tr>
<td><strong>Start-up mech.</strong></td>
<td>Trfr.*</td>
<td>PoR</td>
<td>L.T**</td>
<td>CP</td>
<td>PoR</td>
</tr>
<tr>
<td><strong>Typical ESR (Ω)</strong></td>
<td>5</td>
<td>--</td>
<td>6.2</td>
<td>--</td>
<td>Up to 450</td>
</tr>
<tr>
<td><strong>Native nMOS</strong></td>
<td>Yes</td>
<td>--</td>
<td>Yes</td>
<td>--</td>
<td>None</td>
</tr>
</tbody>
</table>

*Transformer-based startup scheme; **LC-Tank Oscillator-based clock generator

Conclusions

- A PoR-based Starter is designed for harvesting energy from TEG sources.
- The proposed PoR automatically generate a controlled chain of pulses for startup.
- The proposed PoR disables the Starter after startup to reduce undesirable power.
- The proposed PoR starts up to $E_{SR}$ of 450Ω.
- The min. startup voltage is 170mV with the quiescent starter power of 4nW.