A 9-T Subthreshold SRAM Bitcell with Data-independent Bitline Leakage for Improved Bitline Swing and Variation Tolerance

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Subthreshold Operation

\[ I_D = I_{D0} \frac{W}{L} e^{\frac{V_{GS} - V_{th}}{mV_t}} \left(1 - e^{-\frac{-V_{DS}}{V_t}}\right) \]

• **Advantages**
  - **Ultra-low power**
  - **Minimum energy solution**

\[ P = \alpha \cdot f \cdot c \cdot V_{DD}^2 + I_{leak} \cdot V_{DD} \]

• **Disadvantages**
  - **Small \(I_{on}\)-to-\(I_{off}\) ratio**
  - **Low performance**
  - **Sensitive to PVT variations**
Limitations of 6T SRAM Cell in Subthreshold Operation

- **Stability Failure**
  - Disturbing current reduces cell stability

- **Sensing Failure**
  - Small $I_{on}$-to-$I_{off}$ ratio

- **Write Failure**
  - Weak write path due to PVT variation

- **Limited # of Cells/BL**
  - Large bitline leakage
Previous Subthreshold SRAM Design Techniques

• SRAM Cell Stability Improvement
  – Read disturb-free SRAM bitcells [1][2][3][4]

• Bitline Sensing Improvement
  – Bitline leakage reduction [2][3][4]
  – Sense amplifier redundancy [4]

• Write Margin Improvement
  – Collapsed supply level [2]
  – Boosted wordline voltage [2]

• Bitline Leakage Reduction
  – Stacked devices [2][3]
  – Virtual GND control [4]

Read Bitline Sensing Issue

Conventional 8T SRAM for Low Voltage Operation in 65nm CMOS

- Reduced $I_{on}$-to-$I_{off}$ ratio at lower supply voltage
  - Faster bitline discharging by leakage current
  - Sensing failure due to data-dependent bitline leakage

SRAM cell read current $\gg$ Bitline leakage current
: Successful read

SRAM cell read current $< $ Bitline leakage current
: Read failure
Rationale of Data-independent Bitline Leakage

- Successful bitline sensing is always possible when
  - Cell current $\gg$ maximum bitline leakage
  - Bitline leakage = constant
- Constant bitline leakage always has positive sensing margin
Previous Techniques for Data-independent Bitline Leakage

- **8T SRAM bitcell, ESSCIRC’03**
  - Operation failure in subthreshold region

- **10T SRAM bitcell, ISSCC’07**
  - Large area overhead (4 more TRs + Nwell)
Proposed 9T SRAM Bitcell

Conventional 8T SRAM bitcell

- Cell current for data ‘0’
- Leakage current for data ‘0’

Proposed 9T SRAM bitcell for data-independent bitline leakage

- Data-independent pull-up leakage
  - RGND switching for read operation and leakage control
  - Stacked NMOS transistors reduce bitline leakage
  - RBL level where pull-up bitline leakage and pull-down cell current are balanced
Operation of Data-independent Bitline Leakage

- Data-independent pull-up bitline leakage improves bitline voltage swing
  - Negligible discharging speed of data ‘1’
  - Static bitline voltage
Bitline Voltage Swing Improvement

- **Improved bitline voltage swing**
  - 1kcells/BL at 0.25V and 80°C (32cells/BL using 8T)
- **Improved minimum operating voltage**
  - 0.15V for positive RBL swing (0.3V using 8T)
Reduced Bitline Leakage Power

- Read bitline leakage reduction due to RGND control
  - Read bitline leakage reduction > 99%
- No subthreshold current flowing
Enhanced Bitline Sensing Window

- No bitline discharging for data ‘1’ due to pull-up leakage
- Wider bitline sensing window
- Improved sensing window with leaky corners
Bitcell Layout Comparison

- All TRs using minimum device size
- Area overhead of 5.5%
  - No added Nwell compared to 10T SRAM bitcell [ISSCC07]
  - No additional area for gate contact
Summary

• 9T Subthreshold SRAM bitcell for improving bitline voltage swing and variation tolerance
  – Data-independent bitline leakage to provide positive sensing current
  – 1k cells/BL at 0.25V, 80°C with BL swing of 141mV
  – Enhanced sensing window due to static bitline voltage
  – Less sensitive to process and temperature variations