Reliability study of underfill/chip interface under accelerated temperature cycling (ATC) loading

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Received 22 August 2004; received in revised form 28 January 2005
Available online 17 June 2005

Abstract

Interface reliability issue has become a major concern in developing flip chip assembly. The CTE mismatch between different material layers may induce severe interface delamination reliability problem. In this study, multifunctional micro-moiré interferometry (M3I) system was utilized to study the interfacial response of flip chip assembly under accelerated thermal cycling (ATC) in the temperature range of −40 °C to 125 °C. This in-situ measurement provided good interpretation of interfacial behavior of delaminated flip chip assembly. Finite element analysis (FEA) was carried out by introducing viscoelastic properties of underfill material. The simulation results were found to be in good agreement with the experimental results. Interfacial fracture mechanics was used to quantify interfacial fracture toughness and mode mixity of the underfill/chip interface under the ATC loading. It was found that the interfacial toughness is not only relative to CTE mismatch but also a function of stiffness mismatch between chip/underfill.
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1. Introduction

Flip chip technology is one of the major assembly technologies, with which the smaller packaging can be achieved for a desired functionality. Therefore, flip chip technology is expected to have a rapid growth in the industry applications in the next decade. However, large coefficient of thermal expansion (CTE) mismatch between the chip and the substrate may lead to catastrophic thermal stresses in solder interconnects, and hence reduce life of the package. Epoxy-based underfill materials are, therefore, introduced into flip chip assemblies in order to reinforce the strength of increasingly miniaturized solder interconnects [1,2]. However, during the manufacturing process, low adhesion due to incompatible interfaces or under-cured underfill, and void defects caused by trapped moisture can lead to another serious reliability problem, i.e., interface delamination, in the flip chip assembly [3]. It has been reported that the solder joint fatigue failure appeared shortly after the delamination happens at the interface when the flip chip assembly is subjected to thermal shock testing [4,5]. It is most likely that the crack may initiate at the underfill/chip interface and propagate into the solder joint. The propagation of interface crack will cause the function loss of electronic devices.

Due to the complex nature of flip chip assembly and complicated environmental loading, considerable limitations and difficulties exist in studying the interface...
delamination problem in flip chip packages using traditional strength theory. The most common method used in industry is accelerated temperature cycling (ATC) test, which not only takes a long time and considerable resources, but also gives little insight into the failure mechanism and thus less help in the package design. Accordingly, the research emphasis has shifted strongly to damage and fracture mechanics, which offers a fundamental approach to the delamination problems. Briefly, two categories of research work have been carried out. On the one hand, different numerical and experimental methodologies have been developed to characterize the fracture toughness of polymer/inorganic interface [6,7]. The fracture toughness is employed as a criterion for the interface design. On the other hand, numerical simulations [4,8] and in-situ measurement [9–12] have been performed to investigate the reliability of flip chip assembly subject to different mechanical and environmental loadings. However, less experimental investigation has been conducted on the delamination reliability of polymer/inorganic interface, especially under the real ATC loading due to lack of in-situ/real-time optical measurement system.

In this study, an integrated multifunctional micro-moiré interferometry (M3I) system was developed to measure the deformation of flip chip assembly under the ATC loading. Interfacial fracture mechanics technique was employed to analyze the crack-tip displacement field and further study the interfacial behavior of the delaminated chip/underfill interface. Furthermore, in order to examine the finding of M3I system, an interface fracture mechanics based FEA model was developed to determine the effective interfacial toughness of the assembly under the same temperature loading profile used in the moiré interferometry. The simulation results were found to be in good agreement with the experimental results. Both results showed that the interfacial toughness is not only relative to CTE mismatch but also a function of stiffness mismatch between chip/underfill.

2. Experimental and numerical methodologies

2.1. Moiré interferometry

In this study, an integrated multifunctional micro-moiré interferometry (M3I) system was developed by combining moiré interferometry (MI) technique with phase shifting, micro-force application and measurement, thermoelectric heating and cooling, ultrasonic humidity excitation, and microscopic imaging techniques. The schematic diagram of M3I system is shown in Fig. 1. The system was used to investigate the interface reliability of flip chip assembly. With this system, displacement fields can be determined from moiré fringe patterns

\[
U(x, y) = \frac{N_x(x, y)}{2f},
\]

\[
V(x, y) = \frac{N_y(x, y)}{2f}.
\]

Fig. 1. Schematic diagram of M3I system: (1) computer; (2) driver of phase shifter; (3) microscopic imaging device; (4) phase shifter; (5) moiré interferometer; (6) micro-force controller; (7) micro-force amplifier; (8) cooling chiller; (9) micro-force actuator; (10) six-axis adjustment fixture; (11) miniature thermal cycling chamber (or miniature humidity chamber); (12) chamber support; (13) fixing frame; (14) temperature controller; (15) optical table.
where \( f \) is the frequency of specimen grating, and \( N_i(x, y) \) and \( N_j(x, y) \) are the fringe orders in the \( U(x, y) \) and \( V(x, y) \) field moiré patterns, respectively. In practice, a specimen grating with a frequency of 1200 lines/mm was used. The corresponding contour interval in the moiré fringe patterns was 417 nm/fringe.

2.2. Interface fracture mechanics

For a sandwiched system, as shown schematically in Fig. 2, its solution to plane problems of elasticity depends on two non-dimensional combinations of the elastic moduli, \( K \), and mode mixity \( \psi \). For a sandwiched system, as shown in Fig. 3(b), it consisted of three materials, namely, silicon chip with Si\(_3\)N\(_4\) passivation, underfill and FR-4 with solder mask on top. A commercialized epoxy based underfill material supplied by Loctite\(^\text{\textregistered}\) was used in this study. The composition of the material was 60\% epoxy with 40\% silica filling sizing from 1 \( \mu \)m to 4 \( \mu \)m. The glass transition temperature (\( T_g \)) of underfill was determined to be 105 \( ^\circ \)C using differential scanning calorimeter (DSC) [16].

A specially designed mould was employed to prepare the assembly with desired dimension, i.e., 8 mm (L) \( \times \) 5 mm (W) \( \times \) 1.8 mm (H). The thickness of underfill was determined to be 0.5 mm. In addition, the choice of the underfill thickness optimized for critical adhesion will not result in enhanced resistance to progressive debonding under the temperature cycling load used in this study [17]. To simplify the study, the solder joints were removed since a pre-crack was of difficulty to be prepared at the chip/underfill interface with solder joints existing.

3. Experimental details

3.1. Flip chip assembly

Flip chip assembly studied was shown in Fig. 3(a). In order to simplify the study, the solder joints were removed since a pre-crack was of difficulty to be prepared at the chip/underfill interface with solder joints existing. The attention was drawn on the interfacial delamination behavior between chip/underfill. Since the assembly was symmetric, only half of the assembly was studied, as shown in Fig. 3(b). It consisted of three materials, namely, silicon chip with Si\(_3\)N\(_4\) passivation, underfill and FR-4 with solder mask on top. A commercialized epoxy based underfill material supplied by Loctite\(^\text{\textregistered}\) was used in this study. The composition of the material was 60\% epoxy with 40\% silica filling sizing from 1 \( \mu \)m to 4 \( \mu \)m. The glass transition temperature (\( T_g \)) of underfill was determined to be 105 \( ^\circ \)C using differential scanning calorimeter (DSC) [16].

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A dispenser and a curing oven were employed to prepare the sandwich specimen. By following flip chip packaging process, an optimized curing condition was defined to be 165 \( ^\circ \)C for 8 min. Due to capillary action, underfill was dispensed into the gap between chip and FR-4. When the specimen was partially cured, the

Fig. 2. Interface crack problem.
rubber was quickly removed from the specimen and a sharp crack was fabricated. After molding, each specimen was carefully polished with a fine SiC paper to remove excessive underfill and to obtain the desired dimensions.

3.2. Moiré test

Moiré tests were conducted on the pre-cracked flip chip assembly with the M³I system. The assembly was loaded into the miniaturized thermal cycling chamber. A typical ATC loading was applied onto the assembly. The ATC loading profile is shown in Fig. 4. It had a temperature range of $-40 \degree C$ to $125 \degree C$, a dwell time of 12 min at the two extreme temperatures and a cycle time of less than 65 min. In the experiment, moiré fringe patterns were recorded at different temperature steps, e.g., $-40 \degree C$, $-25 \degree C$, $0 \degree C$, $25 \degree C$, $50 \degree C$, $75 \degree C$, $100 \degree C$ and $125 \degree C$, as depicted in Fig. 4. The platform plotted in the figure showed time for recording fringe pattern images. Based on the moiré fringe patterns, the CTODs around the crack-tip of the assembly can be determined with Eq. (1) and the fracture toughness and mode mixity can be calculated with Eqs. (5) and (6).

4. Numerical simulation

In order to examine the findings of M³I system, a FEA model was established to determine the deformation of the assembly with the same specimen structure, dimensions and temperature loading profile used in the moiré experiment.

4.1. Materials properties

Since the epoxy-based underfill exhibits viscous nature, especially when the temperature is around or above $T_g$, time–temperature-dependent material properties can greatly affect the response of flip chip assembly structure [11]. The viscoelastic material model, which was established in our previous works [18,19], was employed to describe the deformation behavior of the underfill material.

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Fig. 3. Schematic diagram of the assembly to be studied: (a) flip chip assembly and (b) simplified flip chip assembly.

Fig. 4. Schematic illustration of temperature profile used in the ATC test.
\[ E(t) = E_0 + \sum_{i=1}^{I} E_i e^{-t/\tau_i} = E_T(t), \]  

where \( E(t) \) is the relaxation modulus, \( I \) is the number of the Maxwell elements, \( \tau_i \) is the relaxation time related to the \( i \)th Maxwell element, \( E_T(t) \) is the tangent modulus, defined as \( E_T(t) = \frac{d\sigma(t)}{dt} \), which is non-strain-rate related.

The input data were obtained according to algorithm provided by ANSYS, as listed in Table 1, where \( H \) is the activation energy and \( R \) is the ideal gas constant. Meanwhile, silicon chip and FR-4 were modeled as temperature-dependent elastic materials. The details are listed in Table 2.

### 4.2. Modeling

A commercial FE software, ANSYS version 6.1, was employed and a 3D finite element model was built to simulate the package under the ATC test. The assembly without fillet was modeled with the same dimensions depicted in Fig. 3(b). Visco89 elements were used to simulate the assembly with imperfect underfill, as shown in Fig. 5(a). A zoomed-in area around the crack-tip was shown in Fig. 5(b). The smallest mesh size around the crack-tip was 2.5 \( \mu \text{m} \). FR-4 and silicon chip were

### Table 1

Viscoelastic parameters for underfill material

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
<th>Parameters</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>H/R</td>
<td>15644</td>
<td>C_1</td>
<td>0.264</td>
</tr>
<tr>
<td>CTE (ppm/°C)</td>
<td>Below ( T_g )</td>
<td>T-dependent</td>
<td>C_2</td>
</tr>
<tr>
<td></td>
<td>Above ( T_g )</td>
<td></td>
<td>C_3</td>
</tr>
<tr>
<td>G_{xy}(0) (MPa)</td>
<td>1691.7</td>
<td>( \dot{\epsilon}_1 )</td>
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<tr>
<td>G_{xy}(\infty) (MPa)</td>
<td>23.3</td>
<td>( \dot{\epsilon}_2 )</td>
<td>451</td>
</tr>
<tr>
<td>K(0) (MPa)</td>
<td>4500</td>
<td>( \dot{\epsilon}_3 )</td>
<td>30435</td>
</tr>
<tr>
<td>K(\infty) (MPa)</td>
<td>62</td>
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</tr>
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</table>

### Table 2

Material properties for chip and FR-4

<table>
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<tr>
<th></th>
<th>Young’s modulus (GPa)</th>
<th>CTE (ppm/°C)</th>
<th>Poisson’s ratio</th>
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<tbody>
<tr>
<td>Silicon chip</td>
<td>132.46 – 0.00954( T )</td>
<td>2.113 + 0.00235( T )</td>
<td>0.28</td>
</tr>
<tr>
<td>FR-4</td>
<td>In-plane</td>
<td>24.422 – 0.0226( T )</td>
<td>17.6</td>
</tr>
<tr>
<td></td>
<td>Out-of-plane</td>
<td>10.562 – 0.00957( T )</td>
<td>24</td>
</tr>
</tbody>
</table>

Fig. 5. Finite element model: (a) 3D mesh of sandwich specimen \( z = -0.5 \text{ mm} \) and (b) Mesh zoomed-in at crack front.
modelled as 20-node hexahedron solid95 elements with temperature-dependent properties. Totally, the 3D model had 22,335 elements and 96,800 nodes.

5. Results and discussion

5.1. Moiré fringe patterns under ATC test

Fig. 6 showed typical $U$ and $V$ field moiré fringe patterns around the crack-tip obtained from different temperatures. From the fringe patterns, the thermal deformations at the different temperatures were calculated with Eq. (1). Accordingly, the schematic deformation throughout the whole temperature cycling is shown in Fig. 7. Because of low CTE and high Young's modulus, silicon chip deformed the least compared to the other two materials. It can be observed that, during the heating process, the adherent FR-4/underfill structure behind the crack-tip bent down. The slight loss of warpage was observed in case of dwelling at extremely high 125 °C. It was because of the rubbery or leathery nature of underfill when the temperature was above $T_g$. The coupling between silicon and FR-4 through underfill material tended to diminish and the assembly was in the stress-release state. However, the underfill experienced large inelastic deformation at this state due to large CTE (110 ppm/°C), the large strain would also consequently affect the interfacial reliability.

When the assembly was cooled down to room temperature, the structure lost warpage, but the residual warpage remained in the assembly due to viscoelasticity nature of underfill at high temperature, especially at the temperature loading higher than $T_g$ of underfill (e.g., 125 °C). When the assembly was cooled down to minus temperature, due to the CTE mismatch as well as stiffness mismatch between underfill and FR-4, the warpage of the structure became significant again for the part of coupled underfill and FR-4 component and the magnitude of warpage increased continuously throughout the entire cooling process.

5.2. FEA examination

Figs. 8–10 showed the deformation patterns around the crack-tip of the assembly under the three temperatures of 75 °C under heating process, 50 °C under cooling process and −40 °C under cooling process. It was noted that the displacements attained from FEA were in agreement with those obtained from the moiré test. In addition, the results proved the tendency of deformation described before. It was also an evidence that the viscoelastic properties of underfill and the temperature-dependent properties of FR-4 and silicon wafer modeled in FEA could more realistically describe the thermal deformation of the sandwich flip chip speci-
5.3. Fracture behavior investigation

Note that the Dundur’s parameters change as a function of elastic mismatch between chip/underfill. In case the elastic moduli of the underfill varied significantly when the temperature went up around and even above the \( T_g \), the corresponding interfacial toughness was changed obviously. In the experiment, the CTODs were derived from the moiré fringe patterns representing displacement along the two crack flanks. Typical CTODs of the whole temperature cycling are displayed in Fig. 11. As seen, when the temperature cooled down to the room temperature, the excessive CTODs were found along the crack. The residual deformation was caused by the viscoelastic behavior of the underfill at the high temperature. When the assembly loaded in the minus temperature, the viscoelasticity of the underfill was not significant since the underfill material exhibit elastic characteristic at the low temperature.

In this study, a characteristic length \( l = h_{\text{underfill}} \) valued 0.5 mm was selected as reference length. The selection of \( l \) was within the zone of dominance of the \( K \)-field, i.e., elastic zone of bimaterial, where the variation of \( l \) is negligible even for changes of \( l \) of several orders of magnitude since \( \varepsilon \) is small in the case of Si/underfill interface [15]. With the length \( l \), the nominal SIFs were calculated as function of \( r^{1/2} \) [7]. As shown in Fig. 12, the nominal \( K_1 \) increased when the \( r^{1/2} \) decreased, while the nominal \( K_2 \) almost remain as a constant when the \( r^{1/2} \) decreased. The two nominal SIFs showed an approximate linear relationship with the \( r^{1/2} \). It is reasonable to assume that the deformation field around the crack-tip was dominated by the \( K \)-field, and the linear extrapolation method [20] could be employed to determine the fracture toughness at the crack-tip. By curve fitting, the experimental and FEM results were extrapolated to the \( y \)-axis using straight line, which represented the interfacial toughness \( K_1 \) and \( K_2 \) at the crack-tip. The values of \( K_{\text{eff}} \) and \( \psi \) were then calculated with Eqs. (5) and (6) and the results are plotted in Fig. 13.

During the heating process, it was observed in Fig. 13(a) that the highest value of \( K_{\text{eff}} \) happened at the temperature between 75°C and 100°C rather than 125°C. From Eqs. (2)–(6), it can be seen that changes of \( E^* \) will affect the value of \( K_{\text{eff}} \) [7]. The possible explanation might be that both CTE and stiffness mismatch inside layered structure could significantly influence the deformation and corresponding fracture behaviors. Particularly, in case the temperature went up to the \( T_g \) of the underfill, the underfill is malleable because of the continuing rearrangement of molecular segments, which is influenced by the secondary bonds in the crystalline region. The rearrangement results in the dramatic decrease in Young’s modulus of underfill, and therefore alters the mechanical relationship in the sandwich structure. Mathematically, it is expressed as rapid decrease in \( E^* \) as defined in Eq. (4). Accordingly, SIFs are prone to decrease significantly as the temperature is close to or higher than the \( T_g \) of the underfill. It could be expressed as

- **CTE mismatch factor:**
  \[
  F_1 = f_1(|\text{CTE}_{\text{underfill}}(T) - \text{CTE}_{\text{FR-4}}(T)|),
  \]

- **Stiffness mismatch factor:**
  \[
  F_2 = f_2(|E_{\text{underfill}}(T) - E_{\text{FR-4}}(T)|),
  \]

- **Warpage:**
  \[
  W = g(F_1 - F_2).
  \]

Similarly, the increase of underfill modulus at the minus temperatures was helpful to increase the \( K_{\text{eff}} \). When the temperature cooled down, there was residual \( K_{\text{eff}} \) generated with the comparison of the \( K_{\text{eff}} \) at the same temperature during the heating up process. This residual value was aroused by viscoelastic deformation especially when the temperature exceeded the \( T_g \). The shifted sign of the phase angle during cooling process, as presented in Fig. 13(b), showed alteration of the direction of shear stress inside the specimen.

As aforementioned, \( K_{\text{eff}} \) decreased as stress relaxation happened in the glass transition state of underfill. However, one cannot determine that the most dangerous stage in the thermal cycling was located at the point with

![Fig. 7. Schematic diagram of deformed shape within whole temperature cycling.](image-url)
highest $K_{\text{eff}}$, since the interfacial toughness varies with the mode mixity at the same time [15]. According to the definition of interfacial fracture extension, the expression can be

$$K_{\text{eff}} = K_{\text{eff}}(\psi),$$

$$\psi = \tan^{-1}\left[\frac{\text{Im}(K\lambda)}{\text{Re}(K\lambda)}\right]$$

(9)

where $\psi$ is the mode mixity. From Eq. (9), it can be seen that the value of $K_{\text{eff}}$ becomes a curve with the function of mode mixity $\psi$ rather than an independent point. Thus, referring to the work done by Suo [21], it is known that the smaller phase angle has corresponding smaller $K_{\text{eff}}$ since mode I failure is more fatal than mode II. Apart from mode mixity, it was anticipated that change

Fig. 8. U and V contour map at 75°C during heating up (stage B in Fig. 4).
of material stiffness (modulus) induced by temperature variation would also decrease the interfacial fracture toughness when the phase angle is fixed [22]. In order to examine the possibility of assembly failure, the ratio of effective interfacial toughness $K_{\text{eff}}$ and critical interfacial toughness $K_{\text{Ceff}}$ was introduced to describe the fracture behavior of underfill/chip interface under ATC loading. The data of critical interfacial toughness for the same interface were obtained from our previous study as shown in Table 3 [12]. As a result, the ratio

Fig. 9. U and V contour map at 50 °C during cooling-down (stage H in Fig. 4).
of $K_{\text{eff}}$ and $K_{\text{Ceff}}$ at 75 °C was found to be smaller than that at 125 °C, i.e., $(\frac{K_{\text{eff}}}{K_{\text{Ceff}}})_{75^\circ C} = 0.185 < (\frac{K_{\text{eff}}}{K_{\text{Ceff}}})_{125^\circ C} = 0.2$. This showed that 125 °C was supposed to be the most catastrophic point during the high temperature loading. Similarly, the ratio of $K_{\text{eff}}$ and $K_{\text{Ceff}}$ at −40 °C was determined to be 0.4, which is even greater than the ratio at 125 °C. It implied that it is also possible to induce the crack propagation at −40 °C. Therefore, it is expected that the interface delamination is prone to propagate at the both extreme temperatures, i.e., 125 °C and −40 °C, during the thermal cycling.

Fig. 10. U and V contour map at −40 °C during cooling-down (stage L in Fig. 4).
6. Conclusions

In-situ moiré measurement was carried out to investigate the thermal deformation and interfacial toughness of delaminated flip chip package under the −40 °C to 125 °C thermal loading condition using the M3I system. FEA numerical simulation was applied to verify the experimental results with the consideration of viscoelastic properties of underfill. The results showed good agreement between experiment and numerical simulation results, which indicated that in-situ measurement can well reflect the structure response of flip chip assembly under thermal cycling.

Both moiré and simulation results showed that not only CTE mismatch was a main cause for interfacial delamination, but also stiffness mismatch played important role on structure deformation and consequently fracture behaviors. The coupling effect between CTE mismatch and stiffness mismatch was of importance to be considered in the design and material choices of flip chip manufacturing. Since the interfacial toughness had different mode mixities at different temperatures, it might not be a suitable parameter for assessment of the most dangerous situation for the package. The ratio of effective interfacial toughness and critical interfacial toughness.

![Fig. 11. CTODs at the distance of r/l = 0.3 obtained from moiré experiment for the whole temperature cycle (l = 0.5 mm; referring to Fig. 4).](image1)

![Fig. 12. SIFs obtained at −25 °C as functions of r^{1/2}.](image2)

![Fig. 13. Representative interfacial toughness and phase angle obtained from FEA and moiré: (a) comparison of FEA and moiré with respect to K_{eff} and (b) comparison of FEA and moiré with respect to ψ.](image3)

![Table 3: Fracture toughness evaluation](table1)
toughness needs to be introduced to determine the most dangerous ATC testing condition.

References


